

[illegible]

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Skew Holes

PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	1D PX/URNA, USB	PCB_ID4	EXT PU REV PD	+3VS
GPIO 01	1D STD/EN	PCB_ID6	EXT PU REV PD	+3VS
GPIO 02		MPC_PWR_CTRL#	EXT PU REV PD	+3VS
GPIO 03		SATA_ODD_DA#	EXT PU	+3VS
GPIO[4:5]		EXTTS_SNI_DRV[0:1]_PCH	EXT PU	+3VS
GPIO 06	1D Pwr/Main	PCB_ID7	EXT PU REV PD	+3VS
GPIO 07	1D USB3.0	PCB_ID3	EXT PU REV PD	+3VS
GPIO 08		BT_ON/OFF#	EXT PU	+3VSUS_ORG
GPIO 09	1D Speaker	ONKYO_DET1	EXT PU	+3VSUS_ORG
GPIO 10	1D Sleep & Multi	PCB_ID11	EXT PU REV PD	+3VSUS_ORG
GPIO 11		EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 12		GPIO12	EXT PU	+3VSUS_ORG
GPIO 13		GPIO13	EXT PU	+3VSUS_ORG
GPIO 14		PCB_ID10	EXT PU REV PD	+3VSUS_ORG
GPIO 15		EXT_SMI#	EXT PU	+3VSUS_ORG
GPIO 16	Clear FWD	GPIO16		+3VS
GPIO 17		DGPU_PWROK	EXT PU REV PD	+3VS
GPIO 18		CLK_REQ1#	EXT PU	+3VS
GPIO 19		BBS_BIT0	REV PD	+3VS
GPIO 20	WLAN	CLK_REQ_WLAN#	EXT PU REV PD	+3VS
GPIO 21	17W/35W/45W	PCB_ID8	EXT PD REV PU	+3VS
GPIO 22		WLAN_LED	EXT PD	+3VS
GPIO 23		GPIO23	TEST POINT	+3VS
GPIO 24		GPIO24	EXT PU	+3VSUS_ORG
GPIO 25	LAN	CLK_REQ_LAN#	EXT PU REV PD	+3VSUS_ORG
GPIO 26		CLK_REQ4#	EXT PU	+3VSUS_ORG
GPIO 27		GPIO27	PD	+3VSUS_ORG
GPIO 28		PLL_ODVR_EN	REV PD	+3VSUS_ORG
GPIO 29		GPIO29	REV PU	+3VSUS_ORG
GPIO 30		ME_SUSPWRDNACK	EXT PU	+3VSUS_ORG
GPIO 31		ME_AC_PRESENT	EXT PU	+3VSUS_ORG
GPIO 32		PM_CLKRUN#	EXT PU	+3VS
GPIO 33		HDA_DOCK_EN#	TEST POINT	+3VS
GPIO 34	1D HDMI SKU	PCB_ID2	EXT PU REV PD	+3VS
GPIO 35		CRT_IN#	EXT PU	+3VS
GPIO 36		SATA_ODD_PRSENT#_R	EXT PU	+3VS
GPIO 37		FDI_OVRVLGT	EXT PD REV PU	+3VS
GPIO 38		PCB_ID0	EXT PD REV PU	+3VS
GPIO 39		PCB_ID1	EXT PD REV PU	+3VS
GPIO 40		GPIO40	EXT PU	+3VSUS_ORG
GPIO 41		GPIO41	EXT PU	+3VSUS_ORG
GPIO 42		GPIO42	EXT PU	+3VSUS_ORG
GPIO 43	1D Speaker	HARMAN_DET2	EXT PU	+3VSUS_ORG
GPIO 44		CLK_REQ5#	EXT PU	+3VSUS_ORG
GPIO 45		CLK_REQ6#	EXT PU	+3VSUS_ORG
GPIO 46		CLK_REQ7#	EXT PU	+3VSUS_ORG
GPIO 47		CLKREQ_PEG#	EXT PU REV PD	+3VSUS_ORG
GPIO 48	17W/35W/45W	PCB_ID9	EXT PU REV PD	+3VS
GPIO 49	1D zero Power GND	PCB_ID5	EXT PU REV PD	+3VS
GPIO 50		DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 51		BBS_BIT1	REV PD	+3VS
GPIO 52	1D eDP/LVDS	PCB_ID12	EXT PD REV PU	+3VS
GPIO 53		KB_LED_ID	REV PU	+3VS
GPIO 54		DGPU_PWR_EN	EXT PU	+3VS
GPIO 55		STP_A16OVR	REV PD	+3VS
GPIO 56		CLK_REQ_PEG_B#	EXT PU	+3VSUS_ORG
GPIO 57		WLAN_ON		+3VSUS_ORG
GPIO 58		SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59		GPIO59	EXT PU	+3VSUS_ORG
GPIO 60		DRAMRST_CNTRL_PCH	EXT PU	+3VSUS_ORG
GPIO 61		PM_SUS_STAT#	TEST POINT	+3VSUS_ORG
GPIO 62		SUSCLK	TEST POINT	+3VSUS_ORG
GPIO 63		SLP_S5#	TEST POINT	+3VSUS_ORG
GPIO 64		DGPU_EDID_SELECT#	REV PU	+3VS
GPIO 65		CLK_USB48_CR		+3VS
GPIO 66		GPIO66	TEST POINT	+3VS
GPIO 67		DGPU_PRSENT#	EXT PD REV PU	+3VS
GPIO 68		SATA_ODD_PWRGT	EXT PU	+3VS
GPIO 69		TV_DET	EXT PD	+3VS
GPIO[70:71]		GPIO[70:71]	EXT PU	+3VS
GPIO 72		BATLOW#	EXT PU& TP	+3VSUS_ORG
GPIO 73		CLK_REQ0#	EXT PU	+3VSUS_ORG
GPIO 74		SML1_ALERT#	EXT PU	+3VSUS_ORG
GPIO 75		SML1_DAT	EXT PU	+3VSUS_ORG

EC
IT8587

EC GPIO	Use As	Signal Name
GPA0		PWR_WHITE_LED#
GPA1		BAT_ORG_LED#
GPA2		KEYBOARD_LED#
GPA3		DC_IN_LED#
GPA4		WLAN_RST#
GPA5		CHGCB2#
GPA6		THERM_ALERT#_EC
GPA7		PCH_FLASH_DESCRIPTOR
GPB0		NUM_LED#
GPB1		CAP_LED#
GPB2		THRO_CPU
GPB3		SMB0_CLK
GPB4		SMB0_DAT
GPB5		A20GATE
GPB6		RCIN#
GPB7		PM_RSMRST#
GPC0		CRX0
GPC1		SMB1_CLK
GPC2		SMB1_DAT
GPC3		KSO16
GPC4		AC_IN_OC
GPC5		KSO17
GPC6		BAT1_IN_OC#
GPC7		ME_AC_PRESENT
GPD0		PM_SUSB#
GPD1		PM_SUSC#
GPD2		BUF_PLT_RST#
GPD3		EXT_SCI#
GPD4		EXT_SMI#
GPD5		PM_PWROK
GPD6		FAN0_TACH
GPD7		USBP01_EN
GPE0		VSUS_ON
GPE1		SUSC_EC#
GPE2		SUSB_EC#
GPE3		CPU_VRON
GPE4		PWR_SW#_M
GPE5		USB_OC01#_EC
GPE6		LID_SW#
GPE7		USB_OC2#_EC
GPF0		BAT1_LEARN
GPF1		ME_SUSPWRDNACK
GPF2		PM_PWRBTN#
GPF3		TEST pin
GPF4		TP_CLK
GPF5		TP_DAT
GPF6		H_PECI_EC
GPF7		LCD_BACKOFF#
GP00		HDMI_HPD_M
GP01		NC
GP02		FB_CLAMP_TGL_REQ#
GP06		HDPINT#
GP00		PM_CLKRUN#
GP01		CHGCB0#
GP02		CHGCB1#
GP03		KB_ID
GP04		JACK_IN#
GP05		HDPLOC
GP06		HDPACT
GP10		AD_IINP
GP11		SUS_PWRGD
GP12		ALL_SYSTEM_PWRGD
GP13		VRM_PWRGD
GP14		ADAPT_AD
GP15		BACK_EN_C
GP16		WLAN_ON_EC
GP17		IMON
GPJ0		SLP_MUSIC_EN
GPJ1		BAT_OFF#
GPJ2		OP_SD#
GPJ3		USBSLP_EN
GPJ4		GPU_FB_CLAMP
GPJ5		CTL_FAN
GPJ6		SW_RICRST
GPJ7		LAN_PWR_EN#
GP00		LPC_AD0
GP01		LPC_AD1
GP02		LPC_AD2
GP03		LPC_AD3
GP04		CLK_KBCPCI_PCH
GP05		LPC_FRAME#
GP06		INT_SERIRQ

EC Name	Use As	Signal Name
WRST#		EC_RST#
FSCE#		SCE#
FSCK		SCK
FMOSI		SI
FMISO		SO
KSI0		KSI0
KSI1		KSI1
KSI2		KSI2
KSI3		KSI3
KSI4		KSI4
KSI5		KSI5
KSI6		KSI6
KSI7		KSI7
KSO0		KSO0
KSO1		KSO1
KSO2		KSO2
KSO3		KSO3
KSO4		KSO4
KSO5		KSO5
KSO6		KSO6
KSO7		KSO7
KSO8		KSO8
KSO9		KSO9
KSO10		KSO10
KSO11		KSO11
KSO12		KSO12
KSO13		KSO13
KSO14		KSO14
KSO15		KSO15

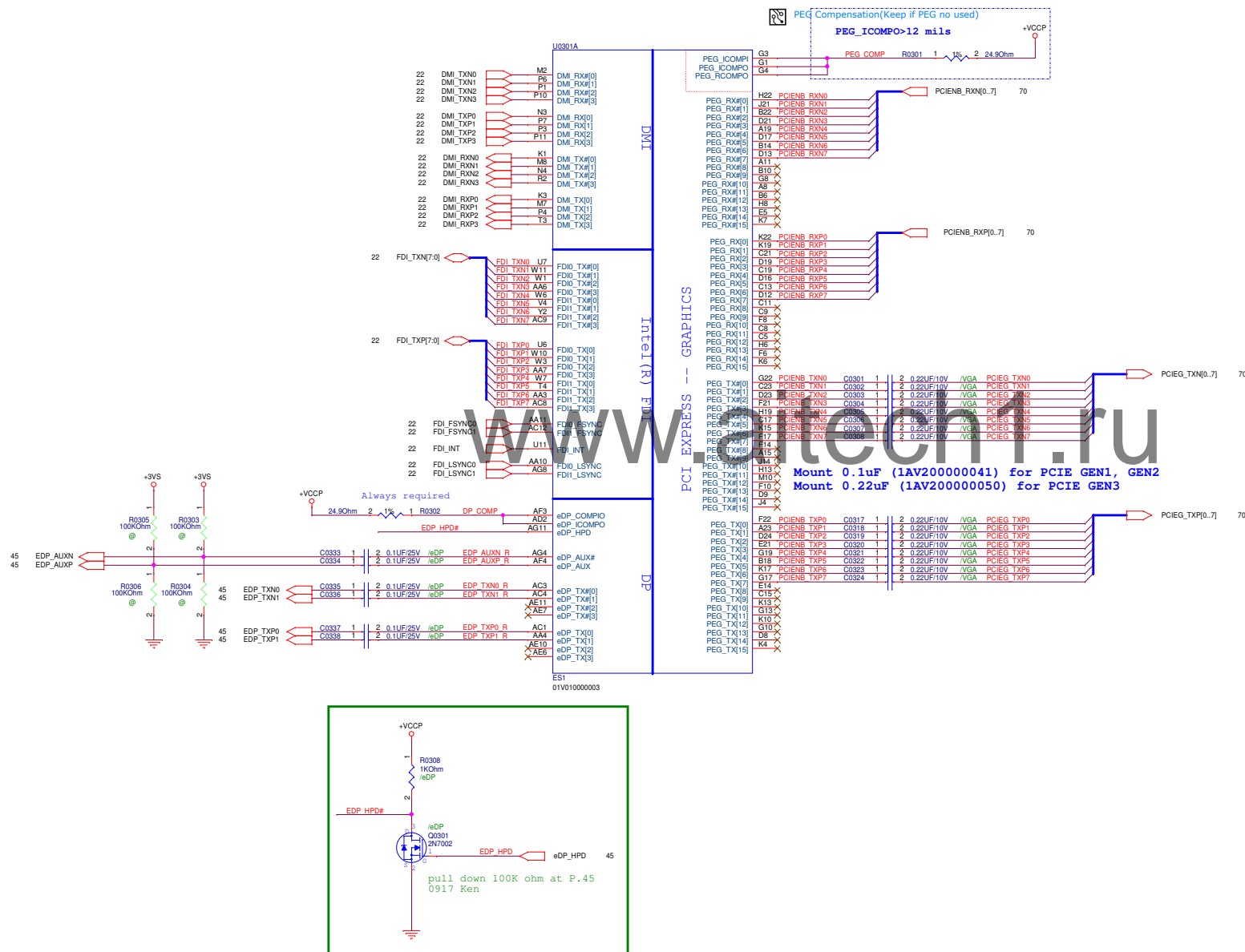
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

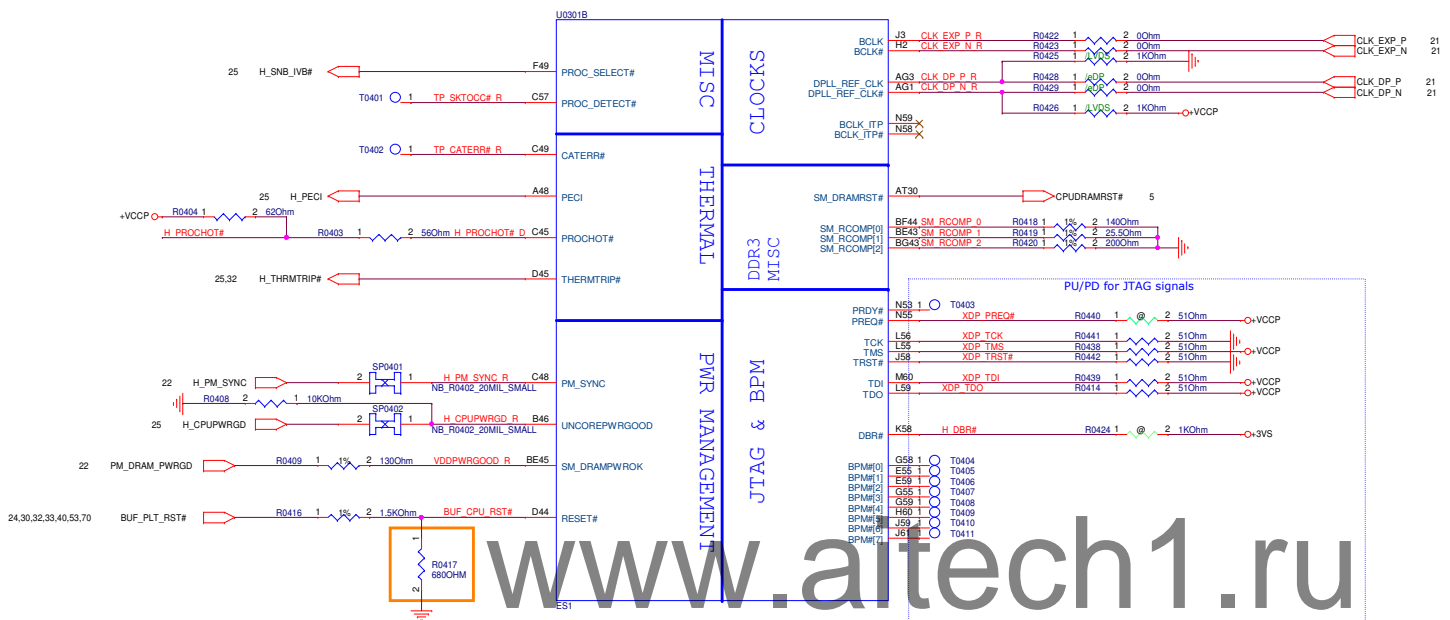
PCIE 1	N/A
PCIE 2	WLAN
PCIE 3	LAN
PCIE 4	N/A
PCIE 5	N/A
PCIE 6	N/A
PCIE 7	N/A
PCIE 8	N/A

USB 0	USB 3.0 Port(Right Front)
USB 1	USB 3.0 Port (Right Back)
USB 2	WiFi/BT
USB 3	USB-Reserve
USB 4	TV Tuner Card1
USB 5	TV Tuner Card2
USB 6	N/A
USB 7	N/A
USB 8	Card reader
USB 9	USB(Left Front)
USB 10	Camera
USB 11	Touch Panel
USB 12	N/A
USB 13	N/A

SATA0	SATA HDD
SATA1	mSATA
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A



+1.5V		+1.5V	5,7,16,17,18,57,83
+3VS		+3VS	3,16,17,20,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+3VSUS		+3VSUS	22,24,27,28,30,33,34,37,53,62,81,92
+VCCP		+VCCP	3,6,7,26,27,32,57,82
+3V		+3V	24,44,45,57,91

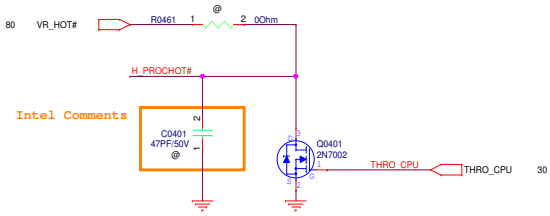


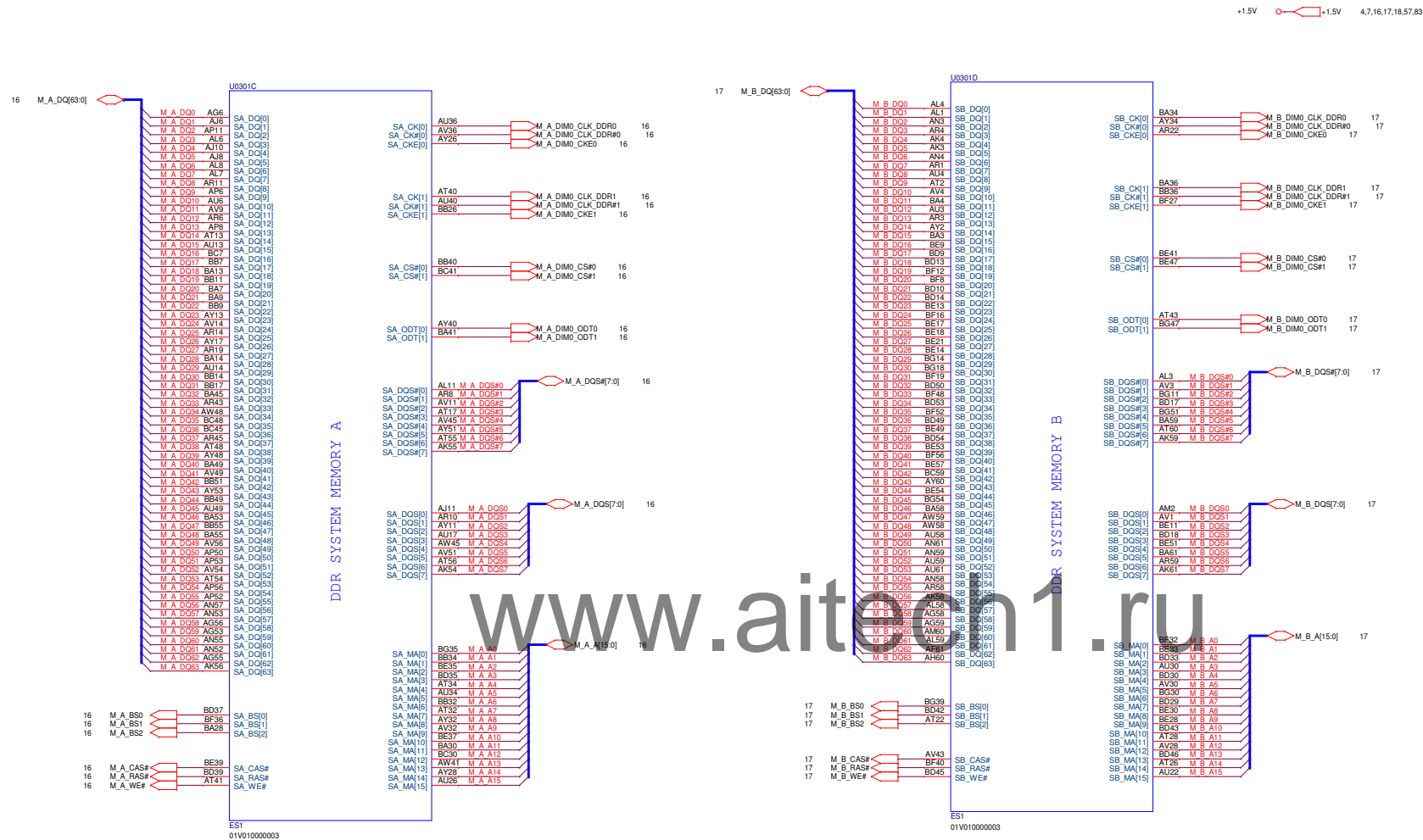
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

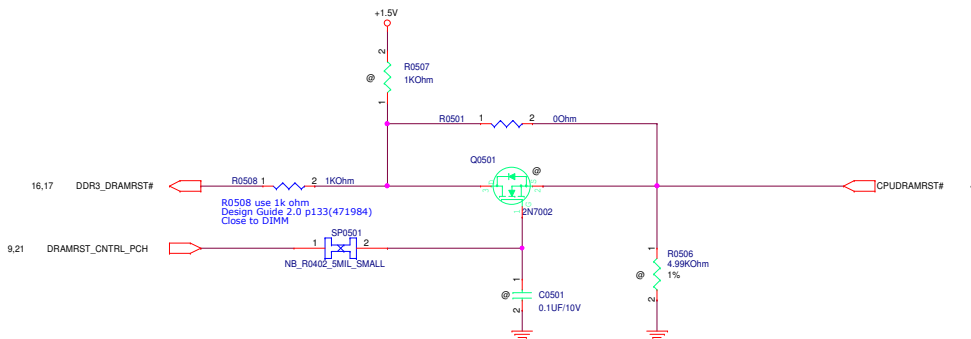
Different from EVEREST

If don't support S3 power reduction
 1. Unmount R0450, R0452
 2. Change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106
 3. Unmount Q0501, C0501, R0506, R0507
 4. Mount R0501, change R0508 to 0ohm from 1kohm
 5. Mount R0702 and short JP0701
 6. Unmount R2232, R2231, Q2203





R1.0 S3 circuit: DRAM_RST# to memory should be high during S3



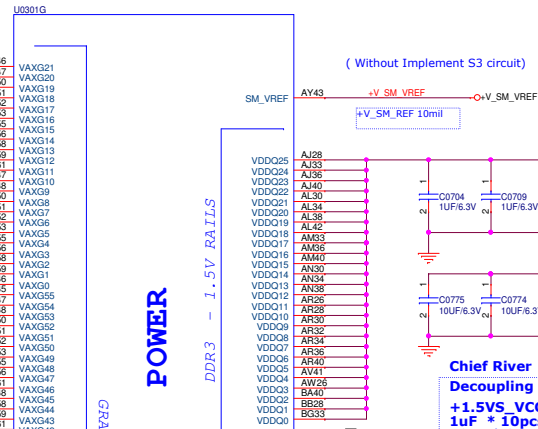
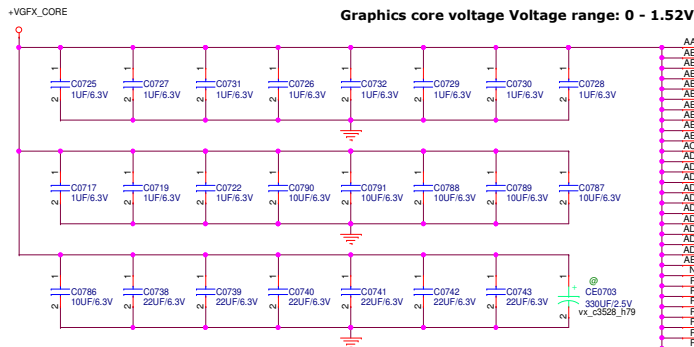
Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS SENSE VCCIO

Chief River
Decoupling guide from Intel (EE)
+VCCP 1uF * 21pcs
10uF * 10pcs
220uF * 1pcs

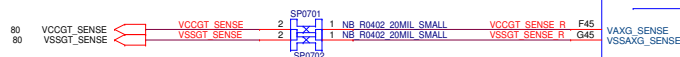
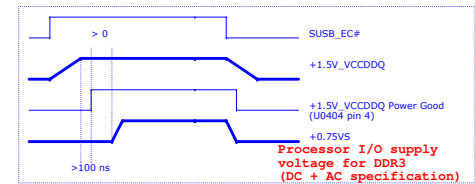


VCCIO_SEL	VCCSA
H	1.05V
L	1.00V

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

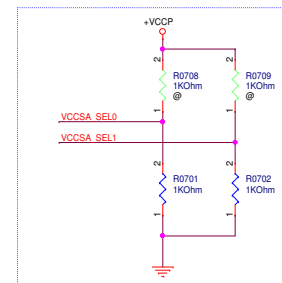
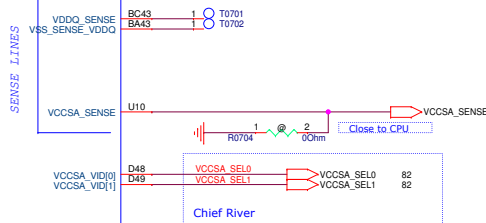
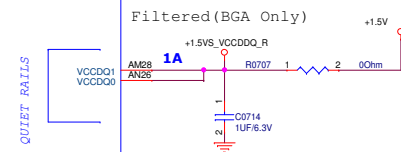


Chief River
Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs

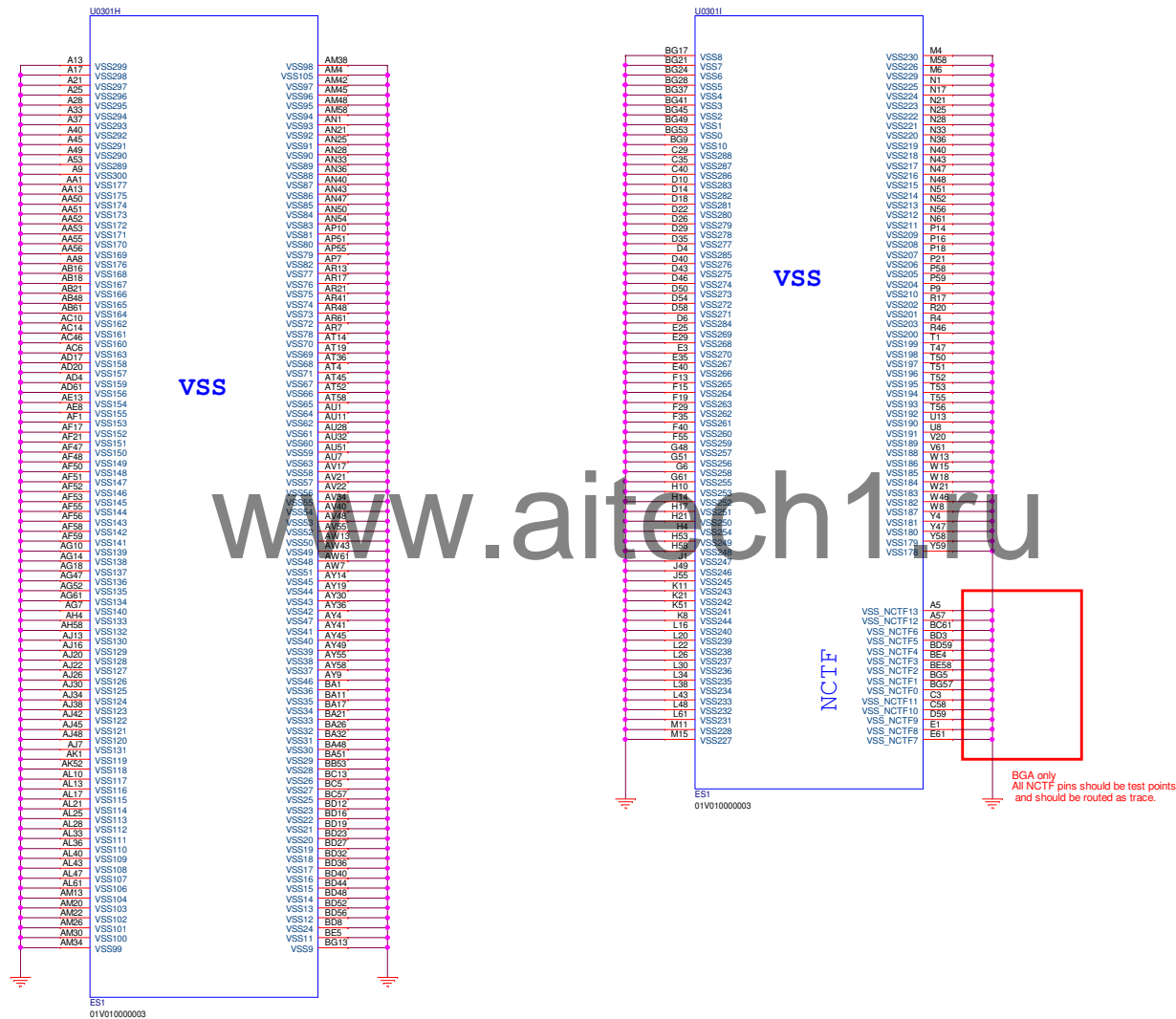


The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It features two main power rails: 1.8V and 2.4V. The 1.8V rail is connected to pin BB3 and includes decoupling capacitors C0761 (1uF/6.3V) and C0764 (1uF/6.3V). The 2.4V rail is connected to pin BC1 and includes decoupling capacitors C0735 (1uF/6.3V), C0736 (1uF/6.3V), C0733 (1uF/6.3V), C0734 (1uF/6.3V), C0737 (1uF/6.3V), C0783 (1uF/6.3V), C0781 (10uF/6.3V), C0792 (10uF/6.3V), C0777 (10uF/6.3V), and C0793 (10uF/6.3V). The diagram also shows the connection of these rails to various pins on the board, including L17, L21, N16, N20, N22, P17, R16, R18, R21, U15, V16, V17, V18, V21, and W20.

Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs



+VCCSA_SELO	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V



CFG strapping information:

CFG[2]: PCIe Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection

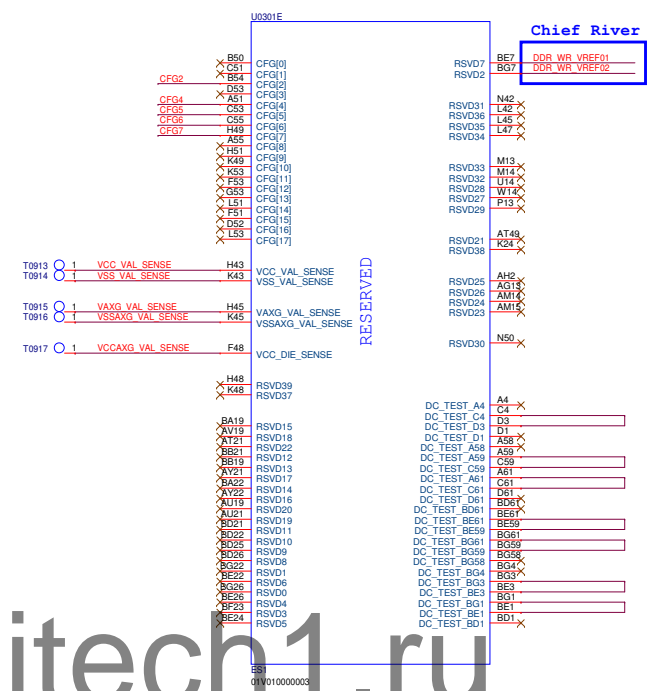
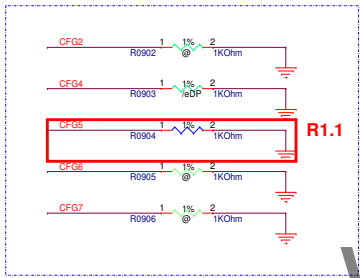
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

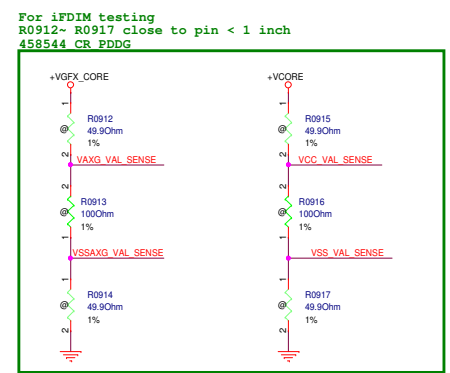
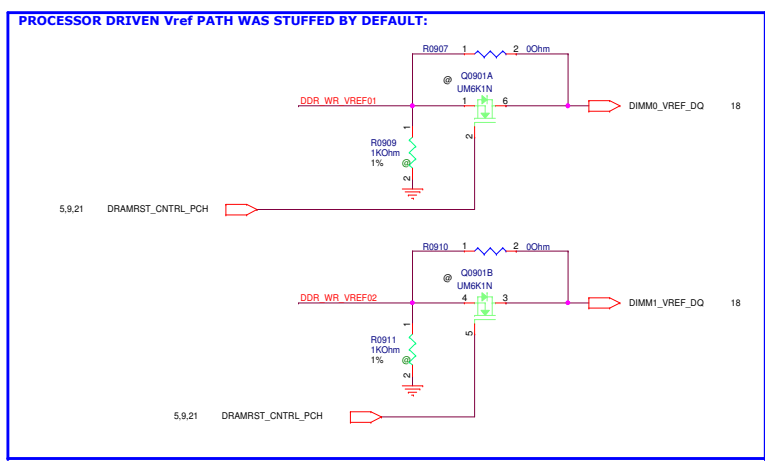
- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



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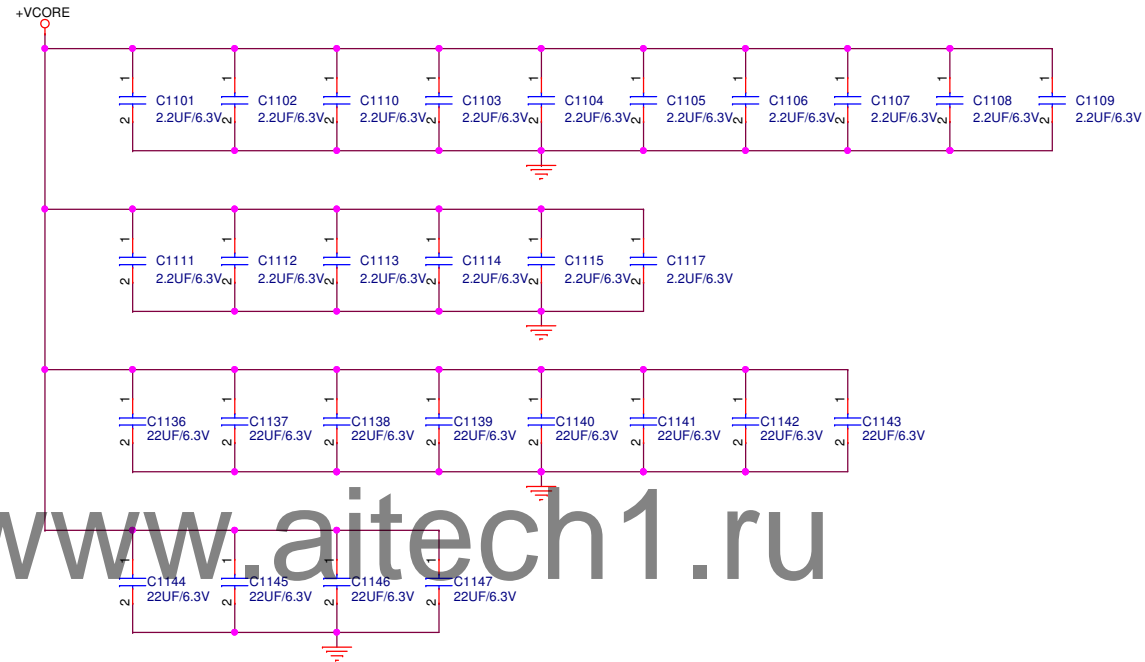
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PEGATRON		Title : CPU_PCH_XDP*****	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size	Project Name		Rev
Custom	VGFTG		1.1
Date: Tuesday, December 11, 2012		Sheet	10 of 104

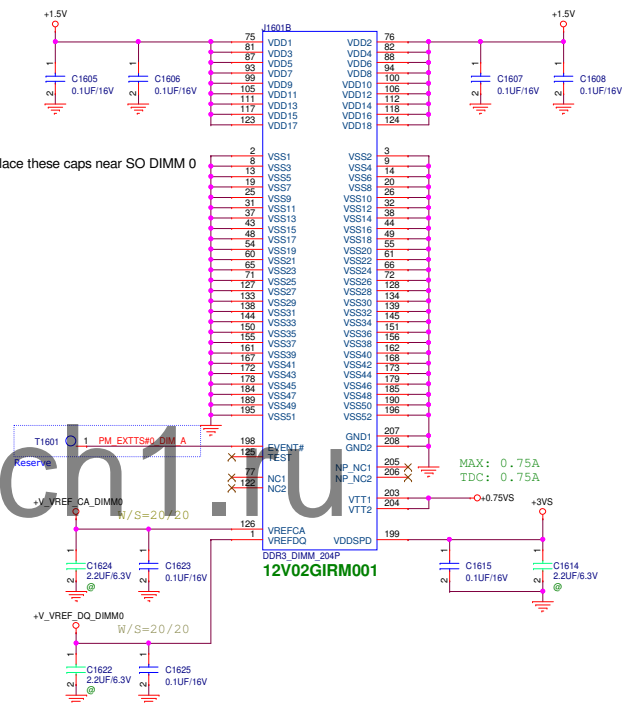
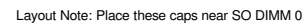
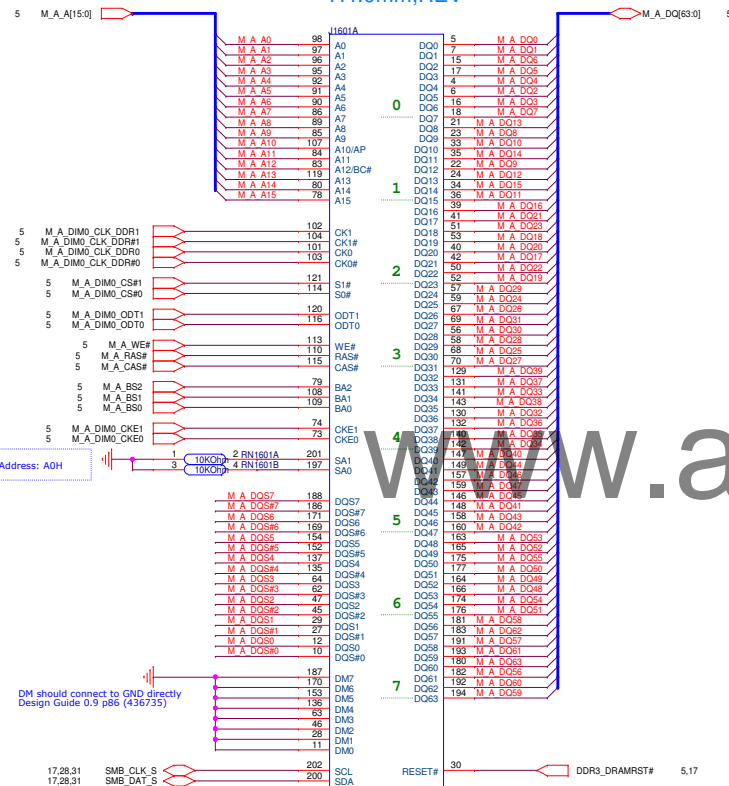
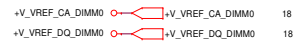
Chief River

Decoupling guide from Intel PDDG R0.8

+VCORE 2.2uF * 16 pcs
22uF * 12 pcs



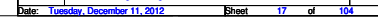
PEGATRON		Title : CPU DECOUPLING	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size	Project Name		Rev
B	VGFTG		1.1
Date: Tuesday, December 11, 2012		Sheet	11 of 104



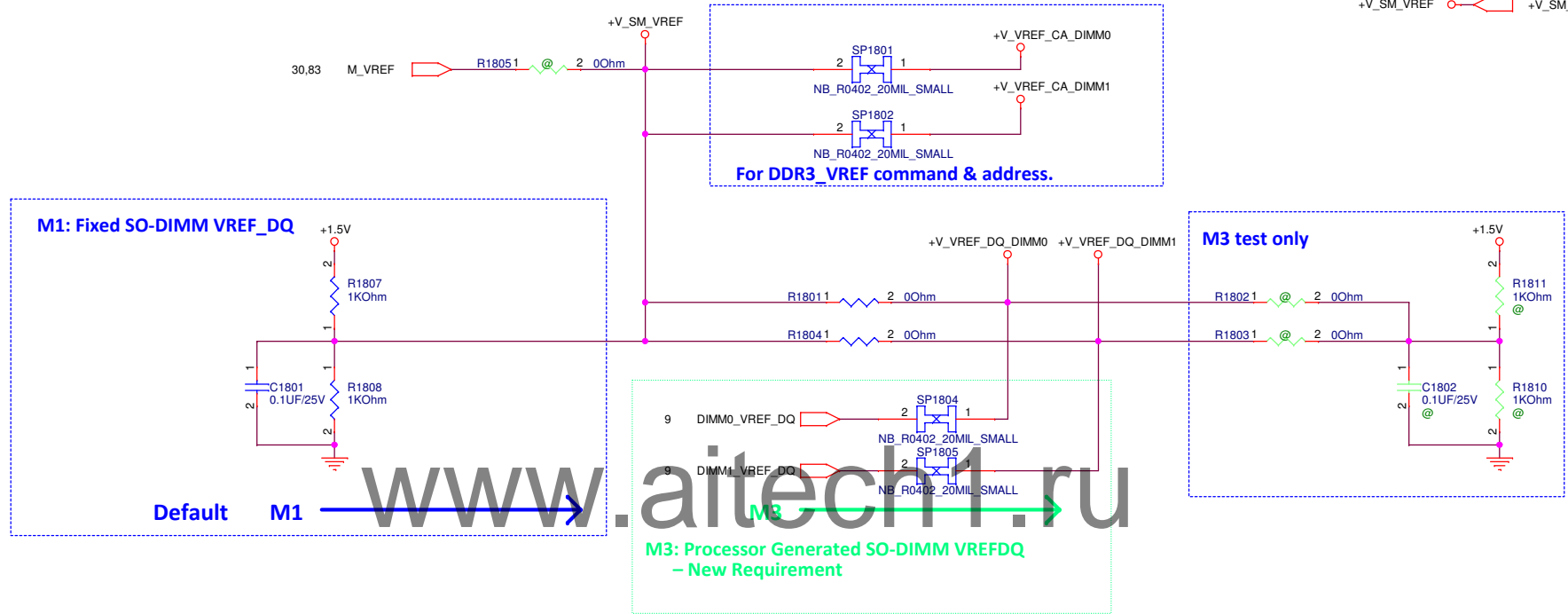
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12V02GIRM001

M: 1202-000R000
S: 1202-00K7000
S: 1202-00LP000



DDR3 Vref



If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

2.WLAN

3.LAN

2.WLAN

3.LAN

U2001B

PCI-E*

SMBUS

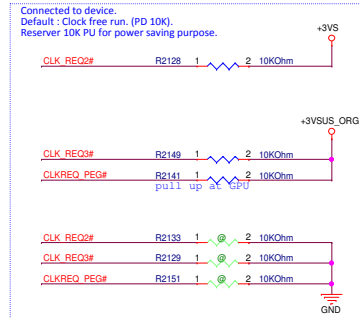
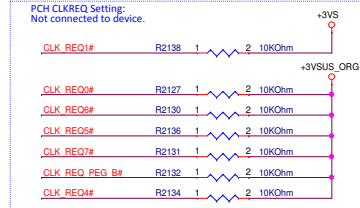
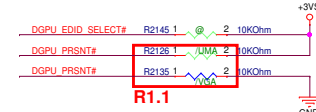
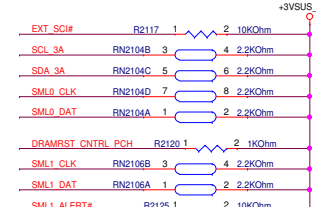
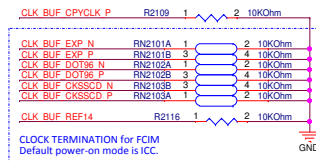
Controller Link

CLOCKS

FLEX CLOCKS

HM70: 0200-00PT0TB
HM76: 0200-00P20TB

+3VS_O 3VS 3,4,16,17,20,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+VTT_PCH_ORG VTT_PCH_ORG 22,26,27
+3VSUS_ORG 3VSUS_ORG 20,22,24,25,27



PEGATRON Title: PCH(2)_PCIE,CLK,SMB,PEG

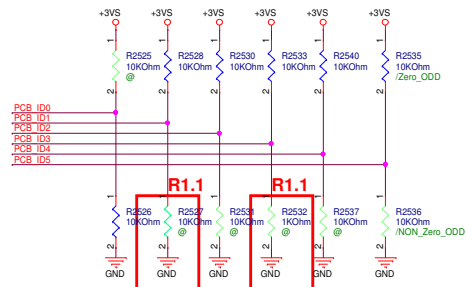
BG1-GSC-HW R&D Dept.5 Engineer: Jim3 Liu

Size Project Name VGFTG Rev

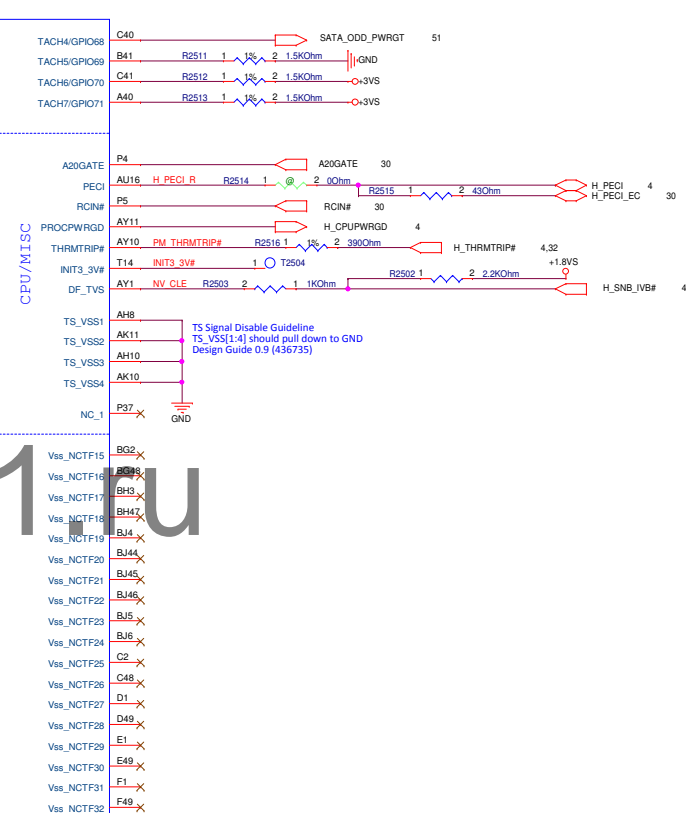
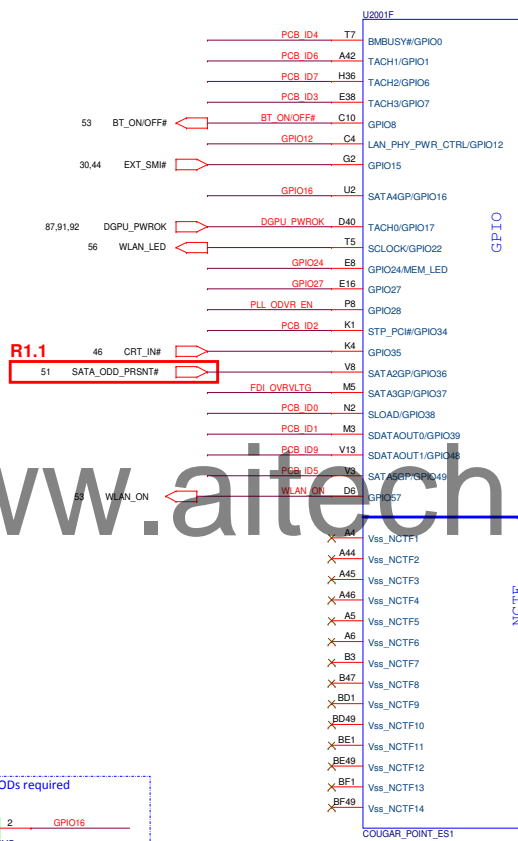
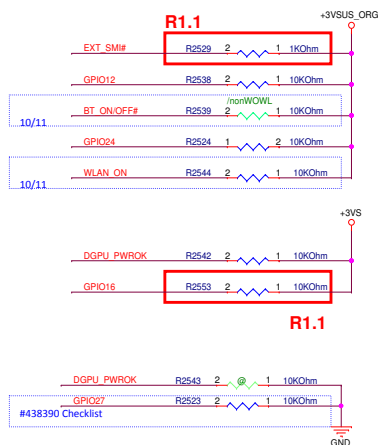
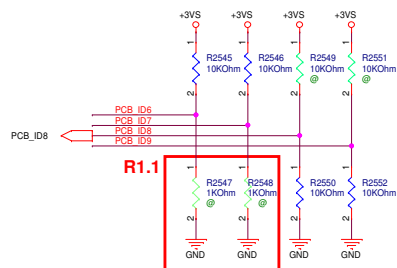
Date: Tuesday, December 11, 2012 Sheet 21 of 104



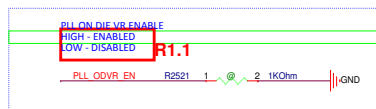
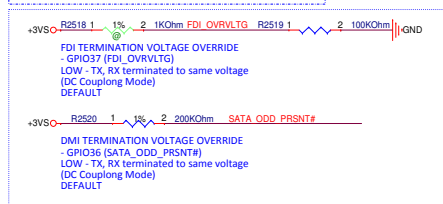
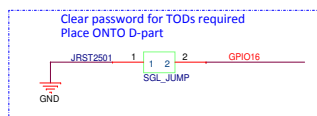
ID0	ID1	PCB Rev.	PCB_ID2	PCB_ID3	PCB_ID4	PCB_ID5
0	0	R1.0	1: HDMI	1: 2 port support	1:OPT/UMA	1:Zero_ODD
0	1	R1.1	0: non-HDMI	0: 1 port	0:DSC	0:NON_Zero_ODD
1	0	R2.0				
1	1	R2.1				

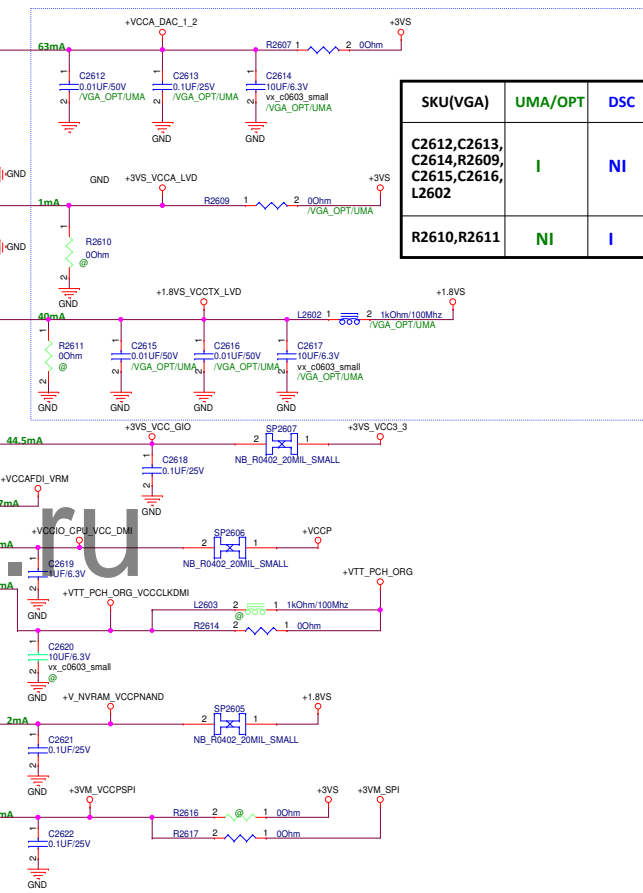
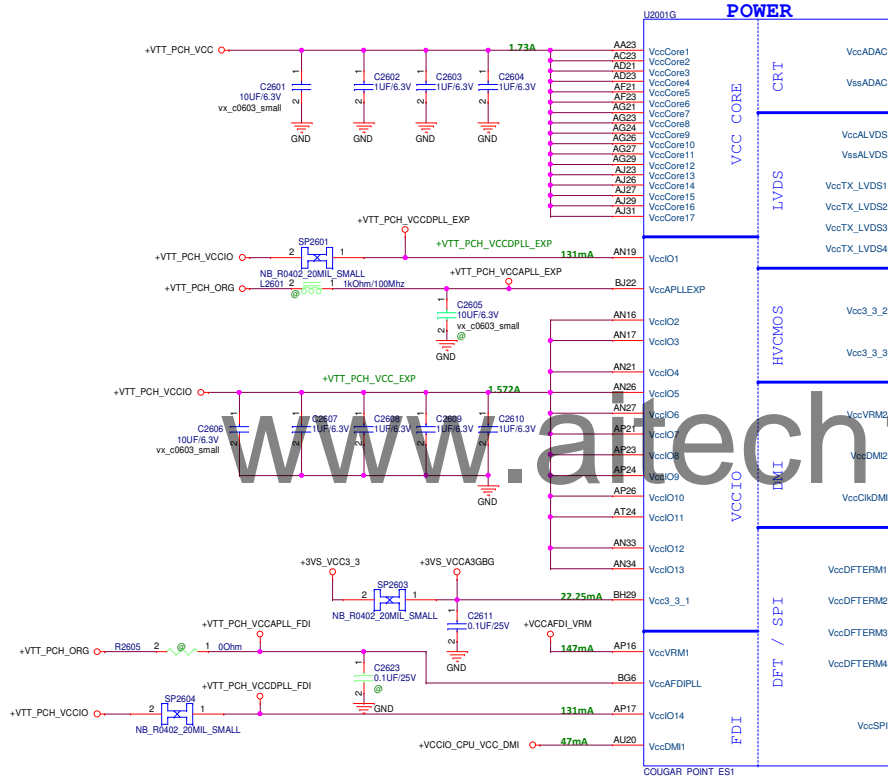


PCB_ID6	PCB_ID7	PCB_ID8	PCB_ID9
1: Standard	1: Premium	0	0: 17W
		0	1: 35W
0: Entry	0: Mainstream	1	0: 45W
		1	1: Reserve



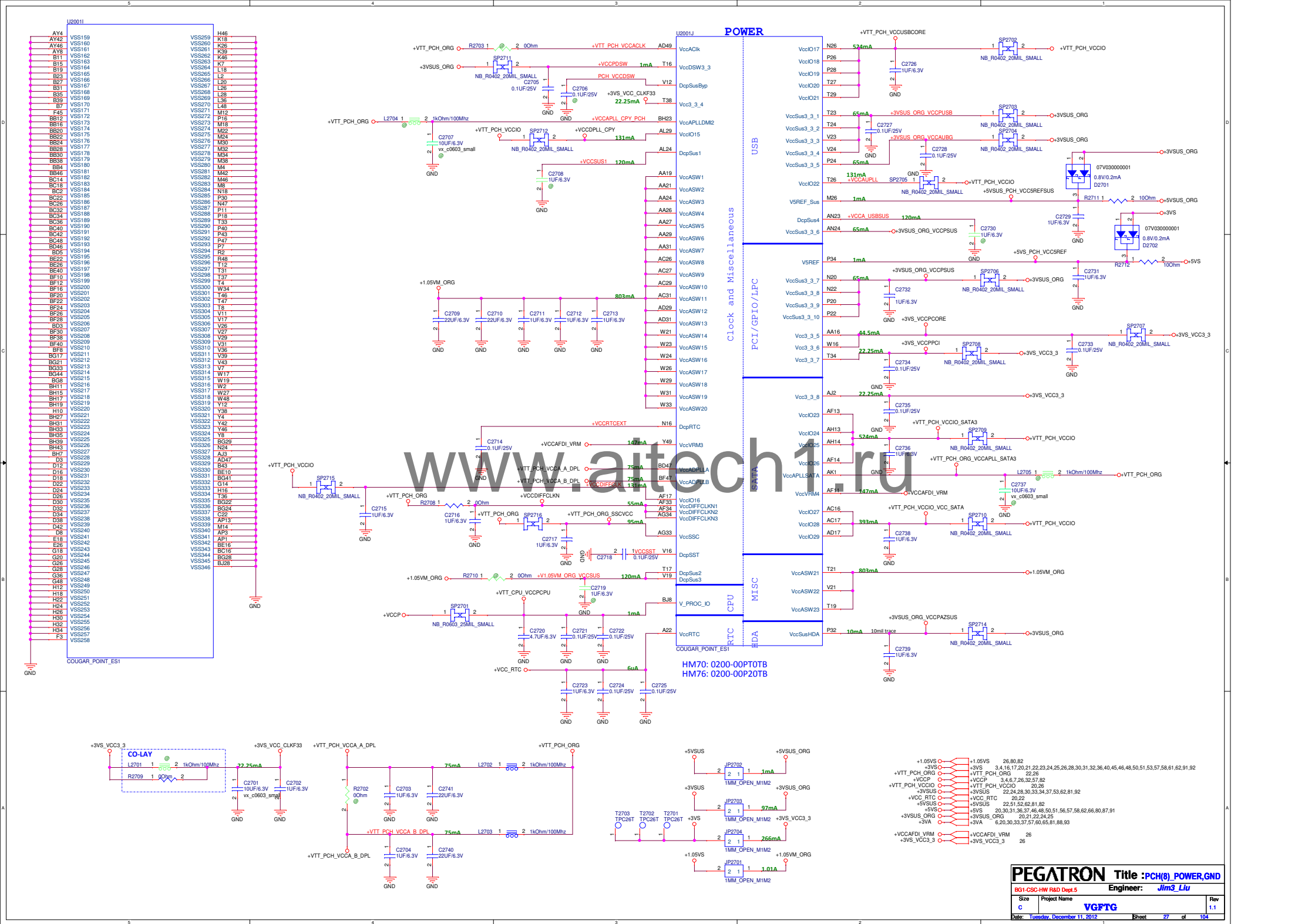
HM70: 0200-00PT0TB
HM76: 0200-00P20TB

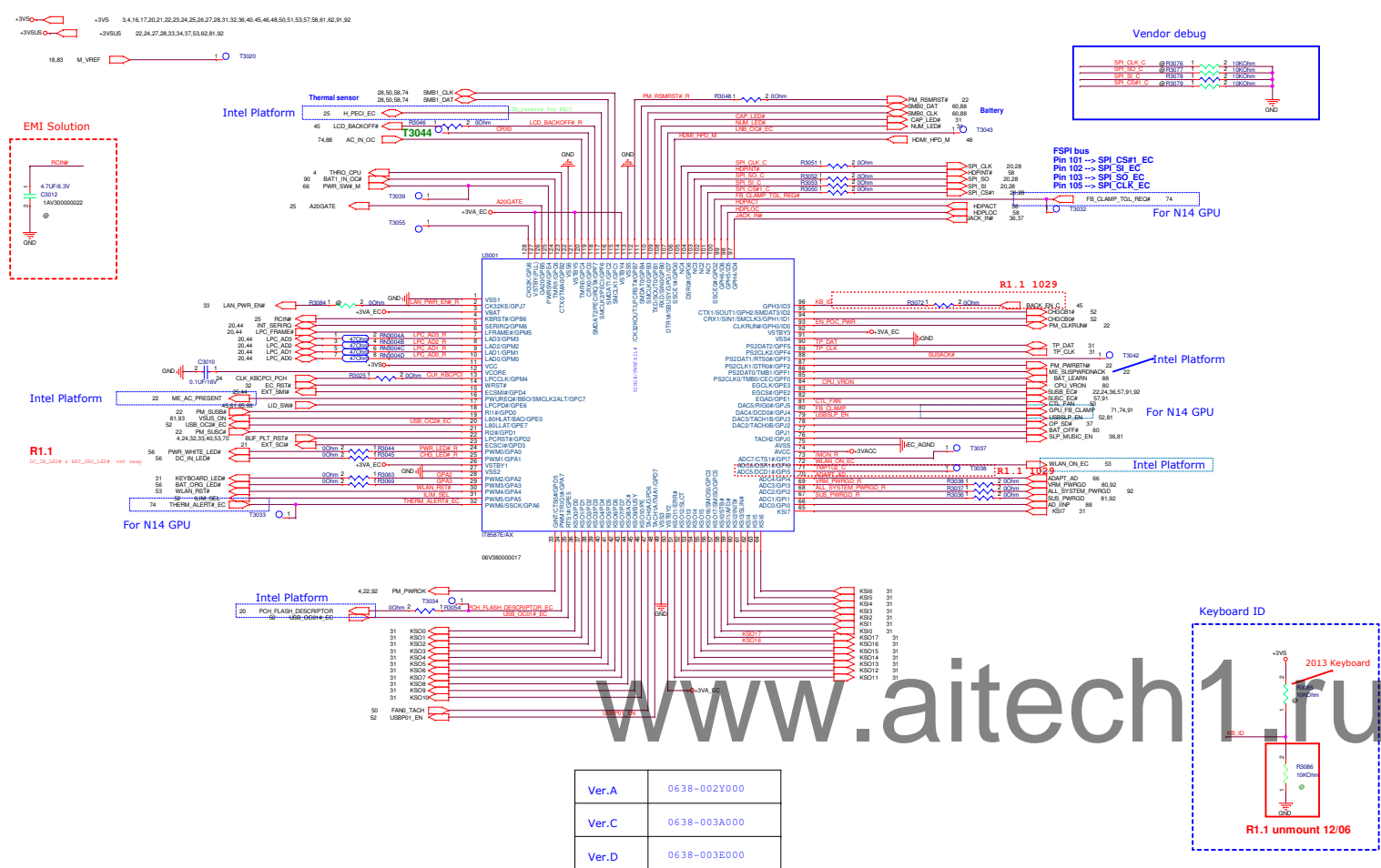




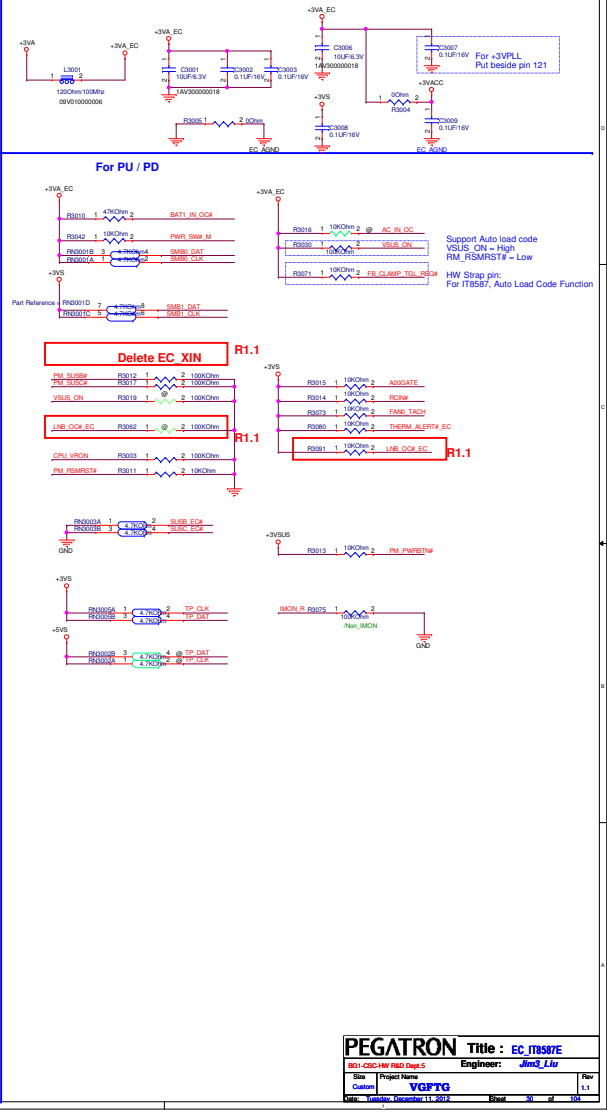
SKU(VGA)	UMA/OPT	DSC
C2612,C2613, C2614,R2609, C2615,C2616, L2602	I	NI
R2610,R2611	NI	I

[illegible]



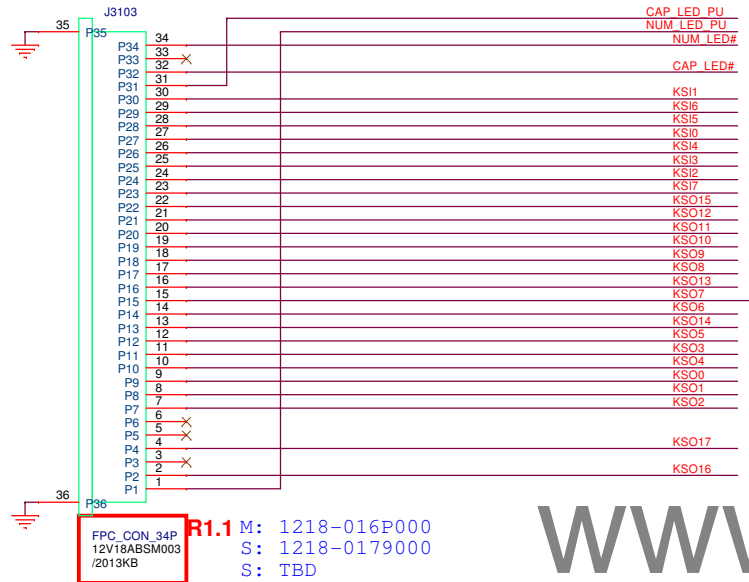


Ver.A	0638-002Y000
Ver.C	0638-003A000
Ver.D	0638-003E000

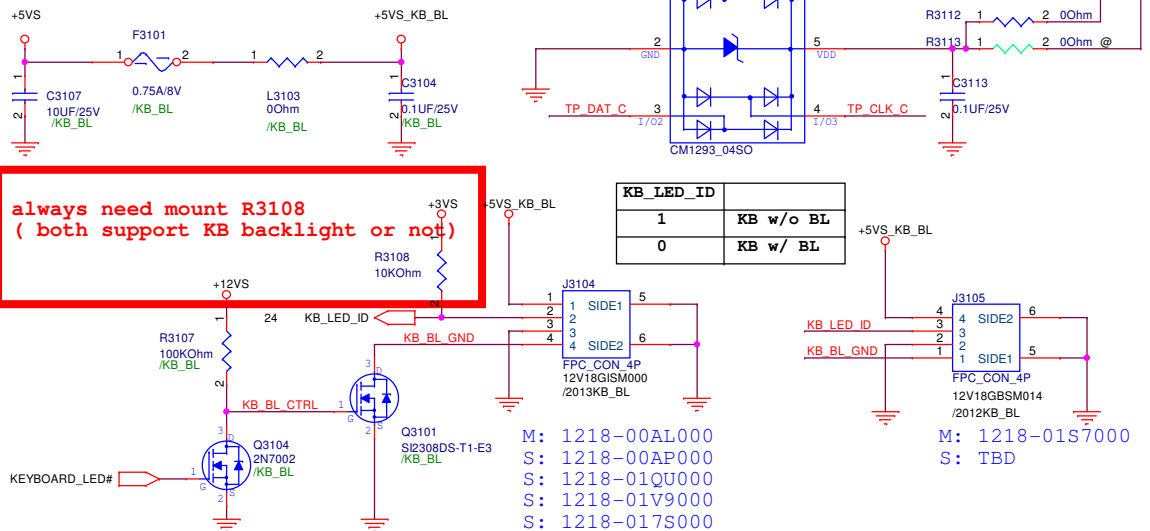


KB CONNECTER

BOTTOM SIDE for 2013 KB



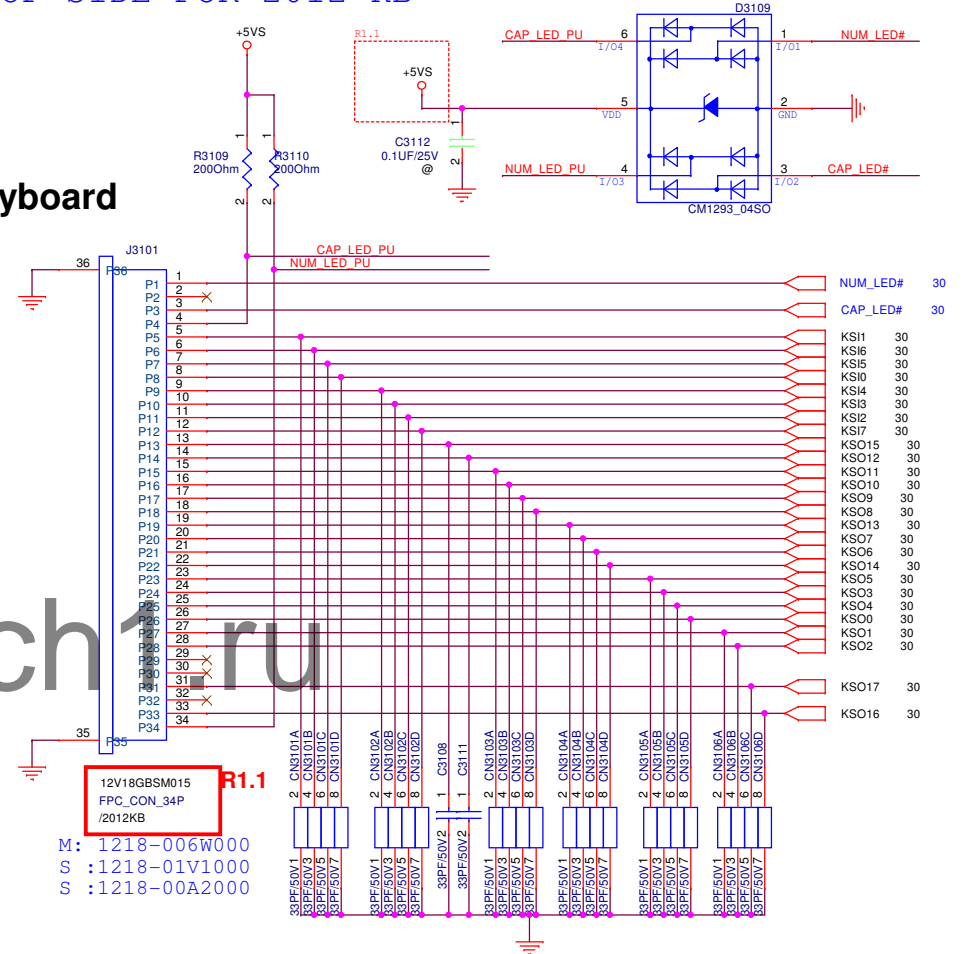
Keyboard LED (暫定)



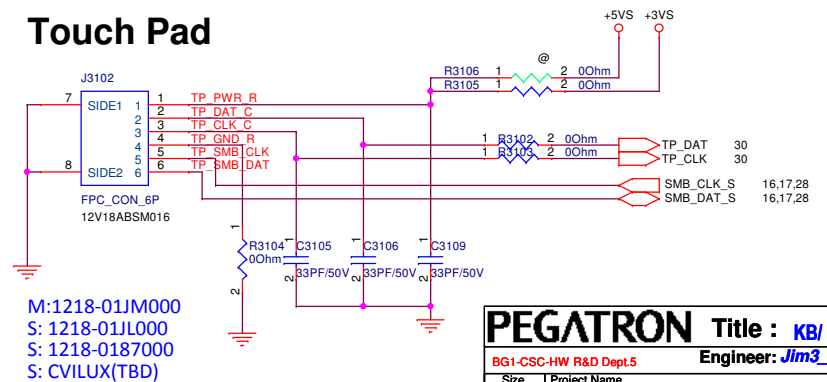
BOTTOM SIDE for 2013 KB

TOP SIDE FOR 2012 KB

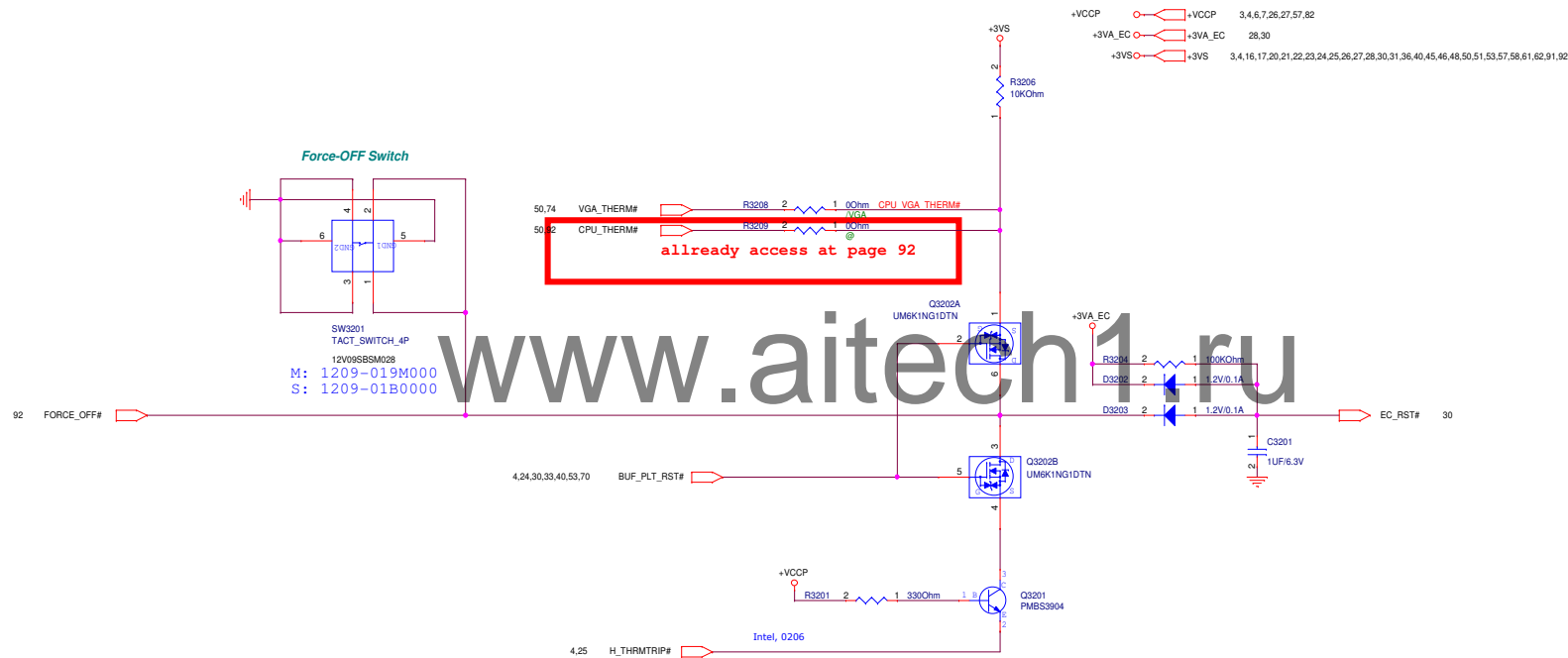
Keyboard



Touch Pad

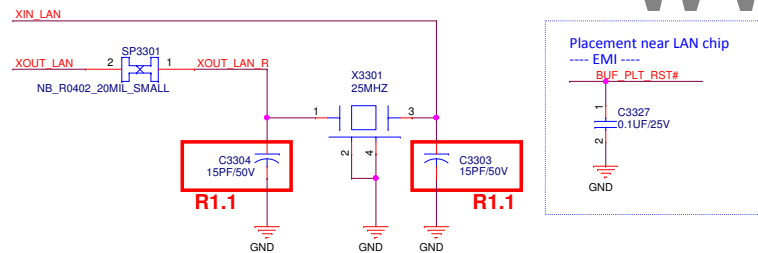
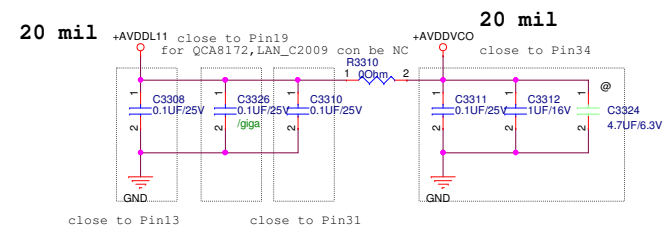
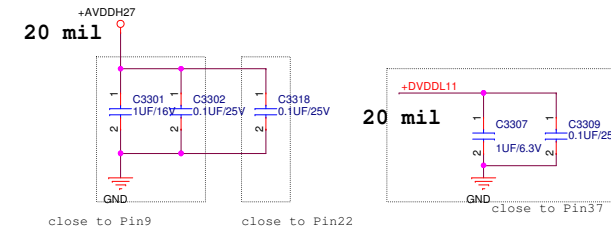


Thermal Policy



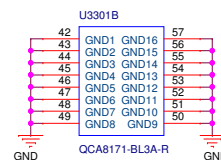
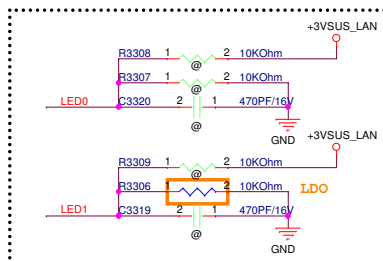
ATHEROS/QCA8171 (gigaLAN)	0200-0040000
ATHEROS/QCA8172 (100LAN)	0200-0041000

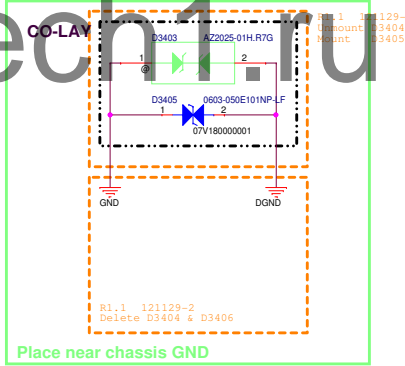
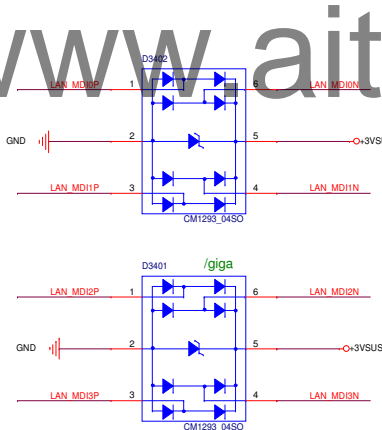
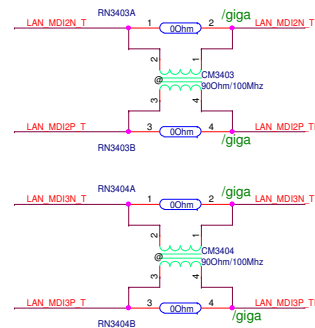
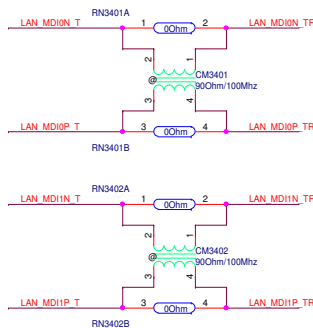
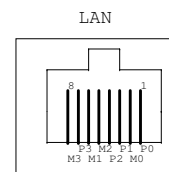
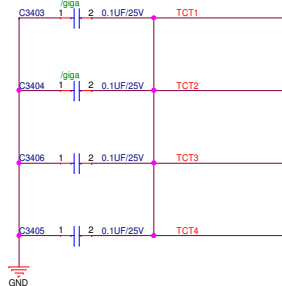
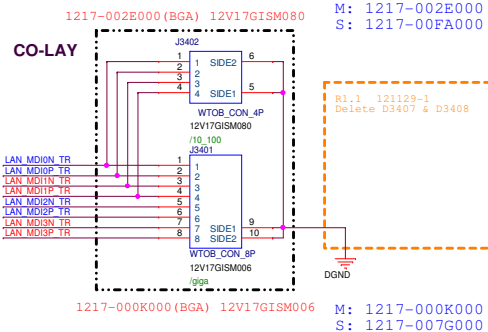
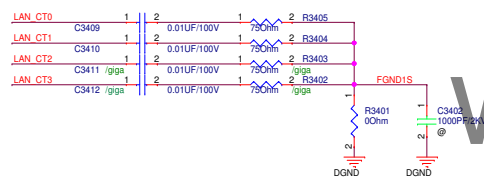
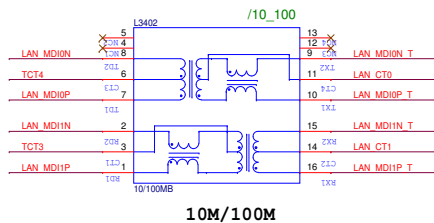
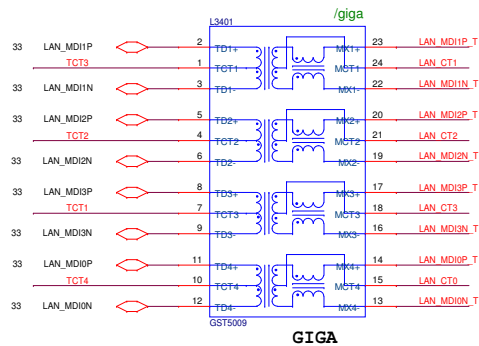
PCIE_TXN_LAN		PCIE_TXN_LAN	21
PCIE_TXP_LAN		PCIE_TXP_LAN	21
CLK_PCIE_LAN		CLK_PCIE_LAN	21
CLK_PCIE_LAN#		CLK_PCIE_LAN#	2

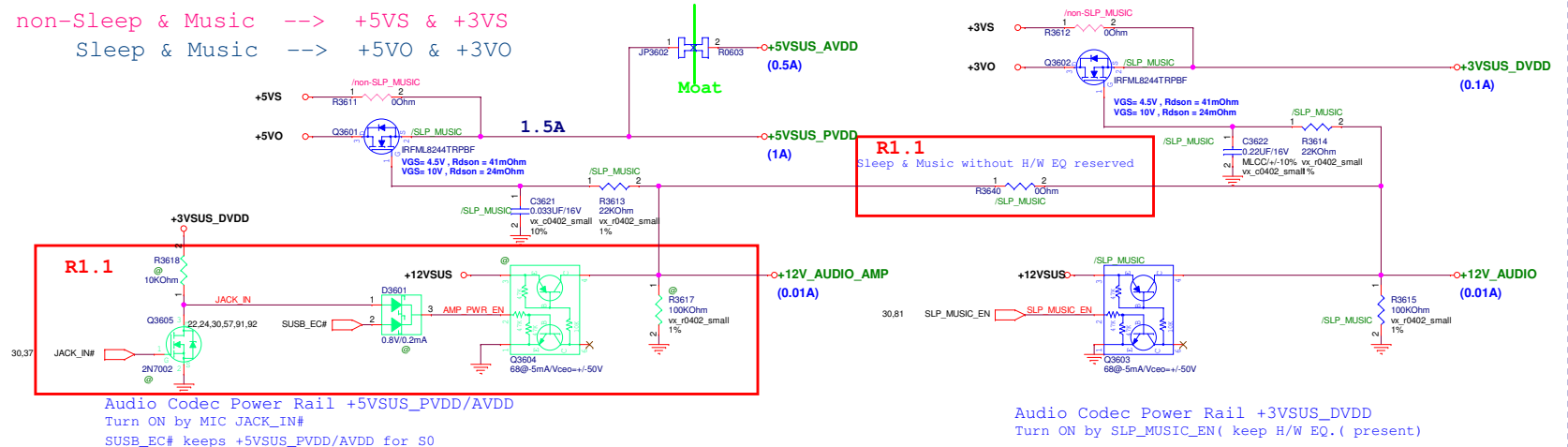
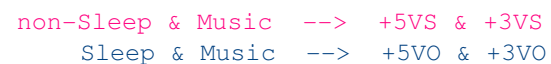
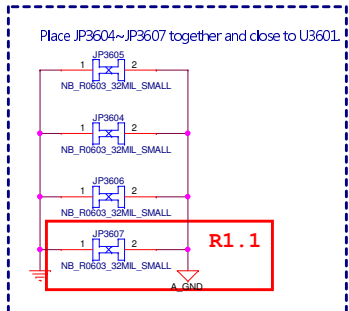
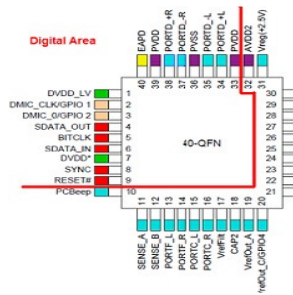
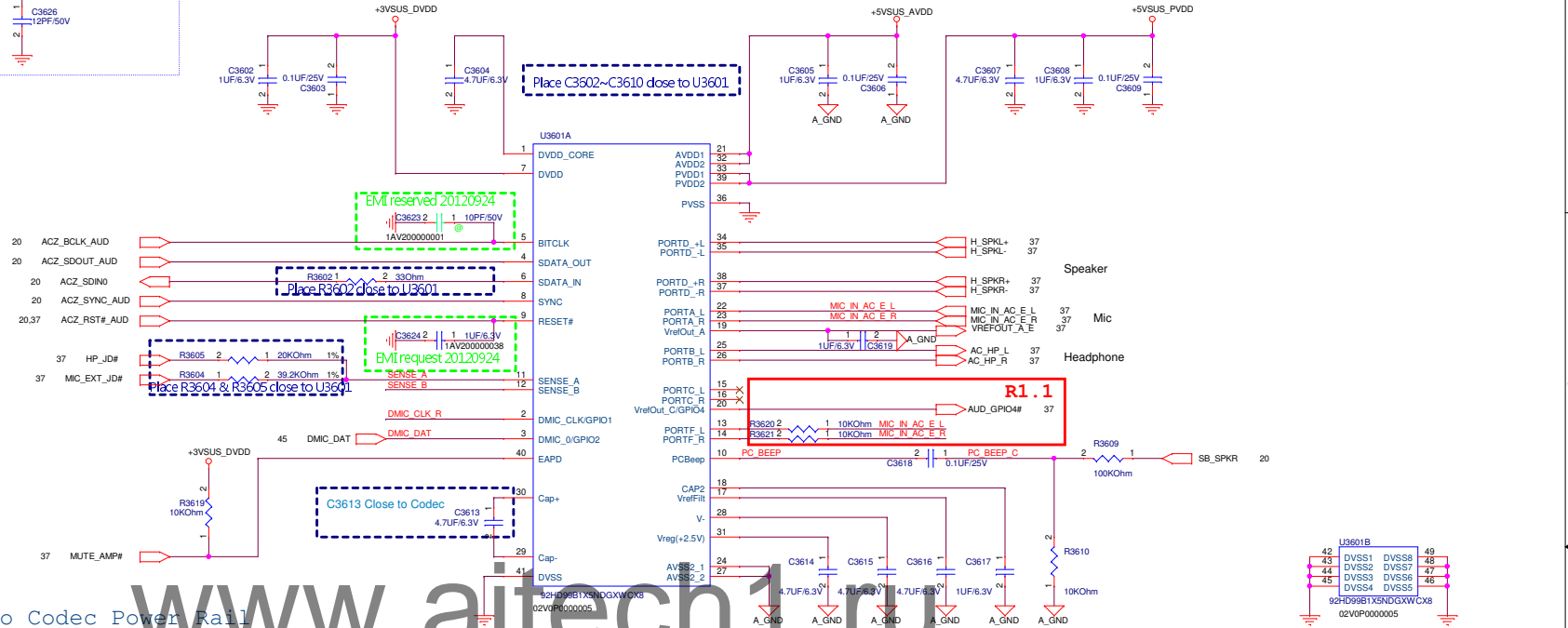
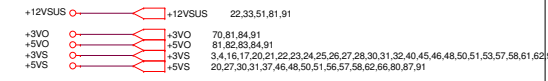
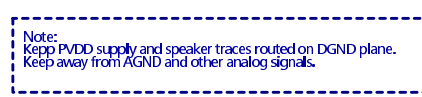
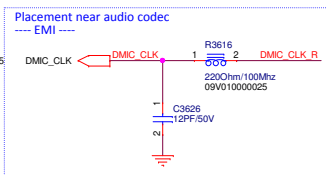
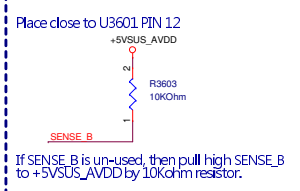
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```
LED[1] -> 1:SWR ; 0:LDO
```

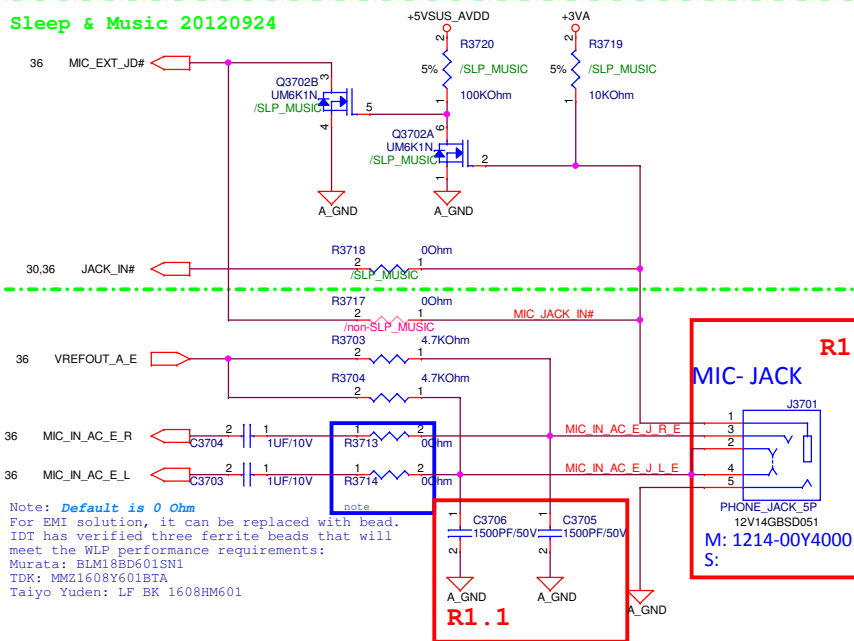
Both LED0 and LED1 with internal pull-high resistors in the chip, LAN_R2006, vR2007, LAN_R2008 and LAN_R2009 must be removed.





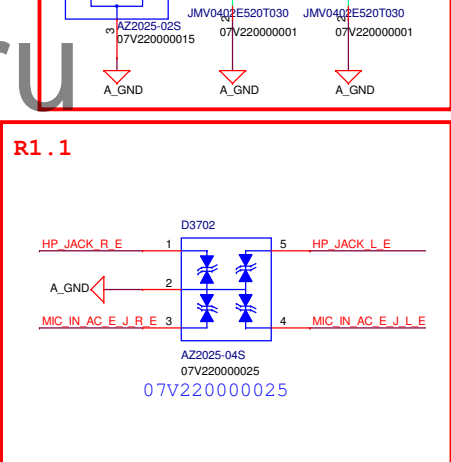
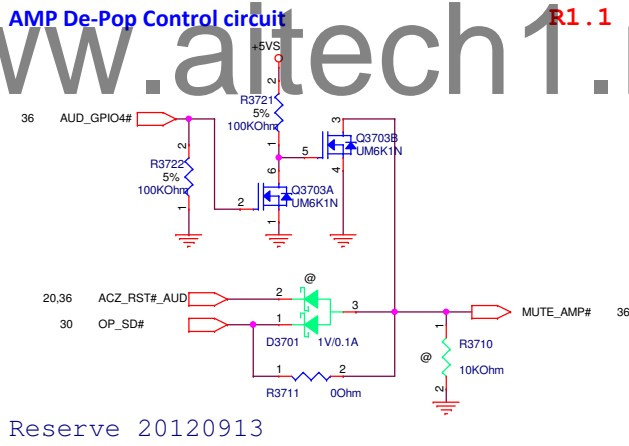
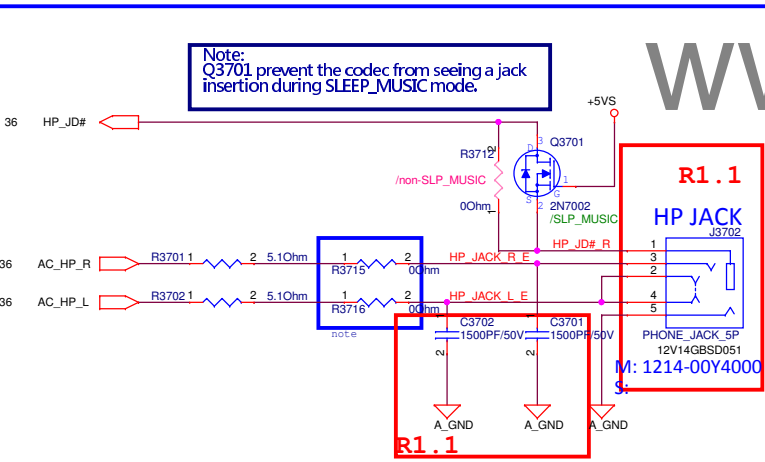
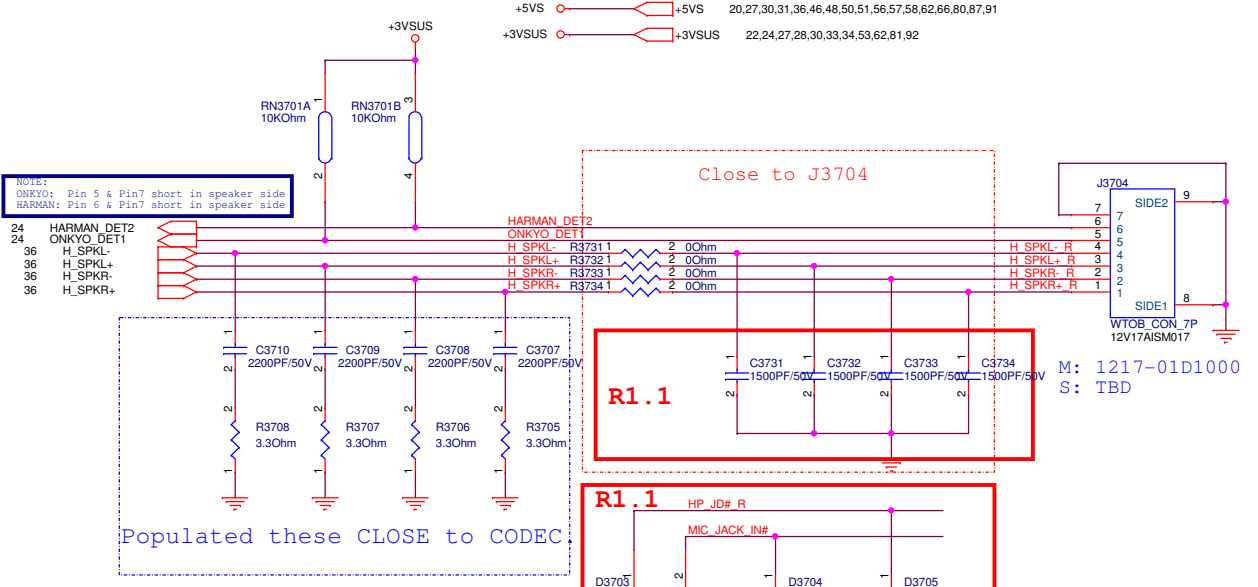


Sleep & Music 20120924



Internal Speakers Header

update speaker header define 20120914

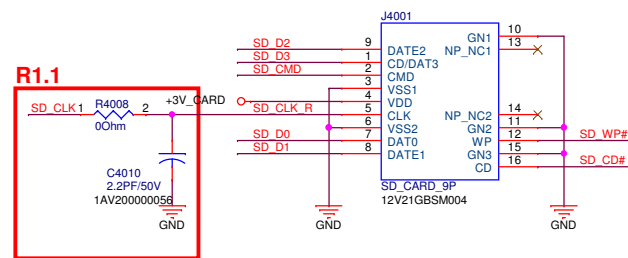
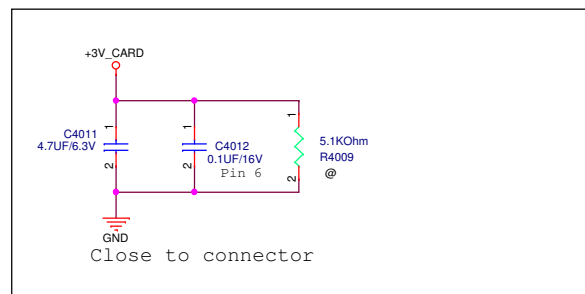


PEGATRON Title :AUDIO_ID92HD99

BG1-CSC-HW R&D Dept.5 Engineer: <Enginner Name>

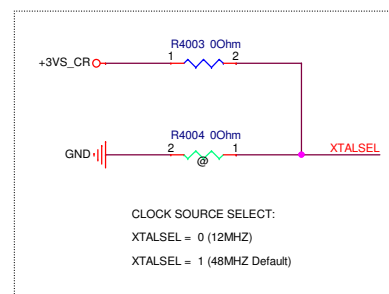
Size	Project Name	Rev
Custom	VGFTG	1.1

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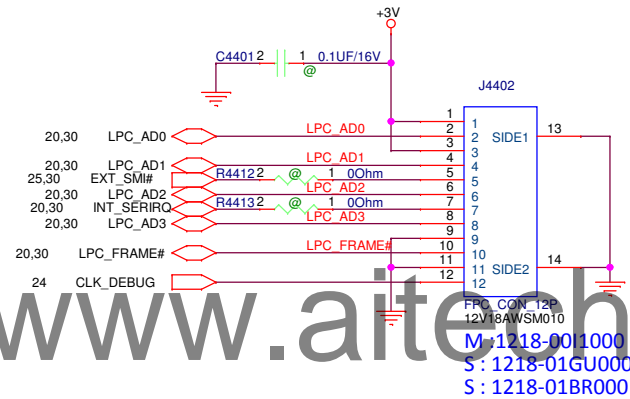
R4008,C4010 Close to connector

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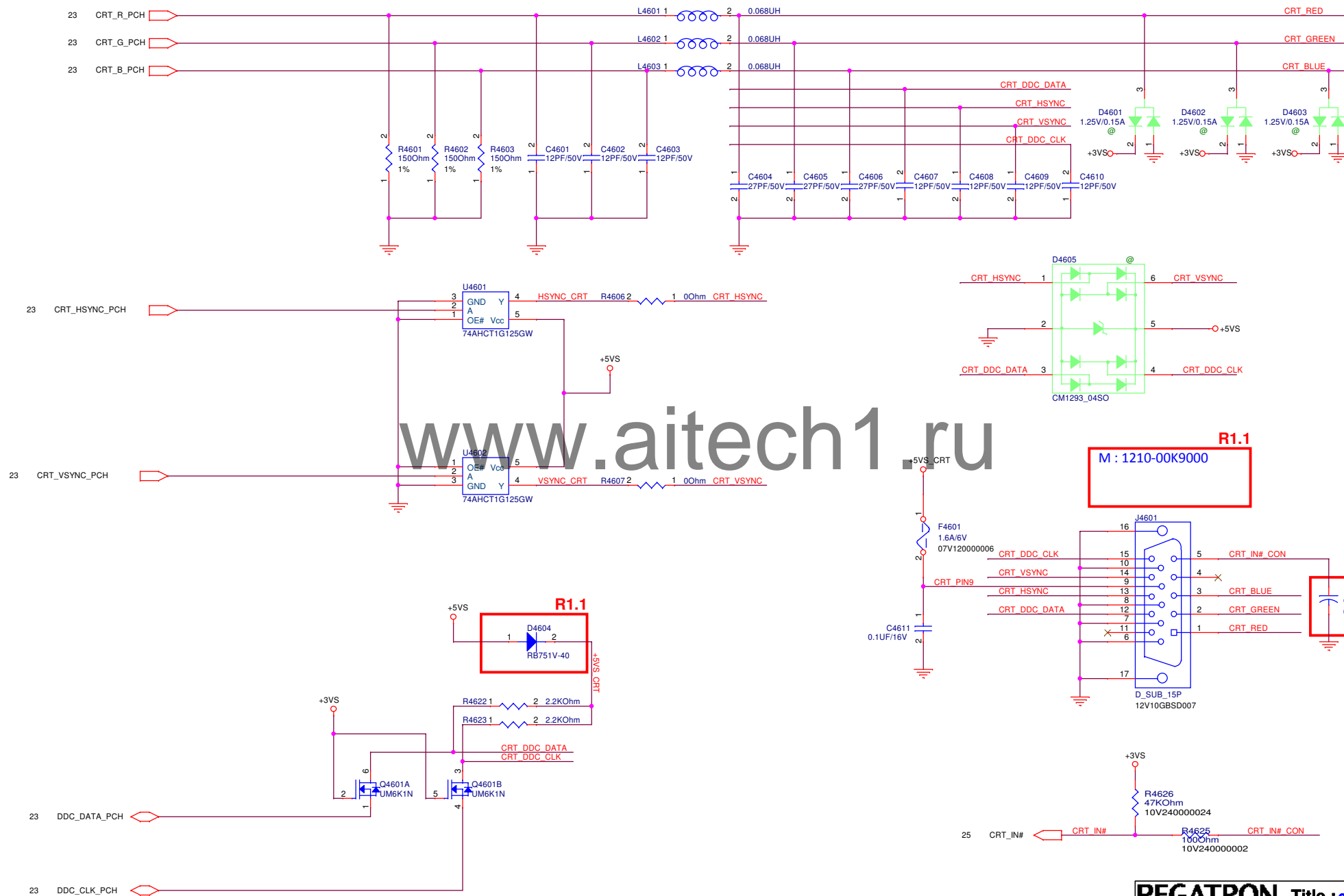


5	4	3	2	1
---	---	---	---	---

DEBUG CARD CONN.

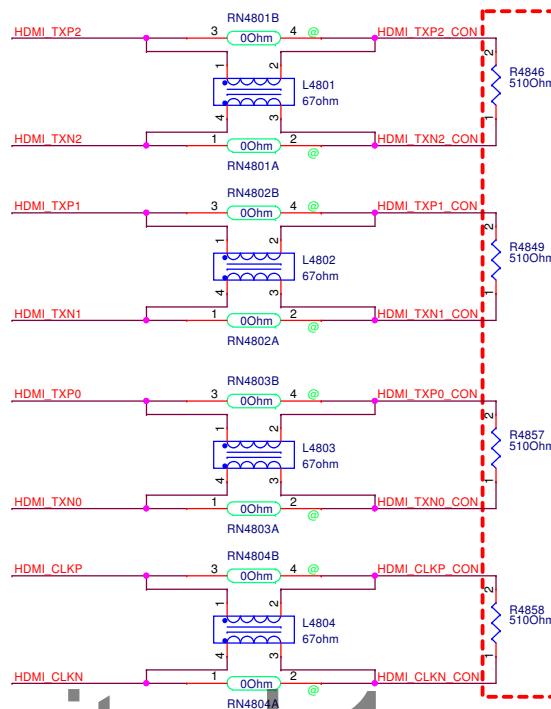
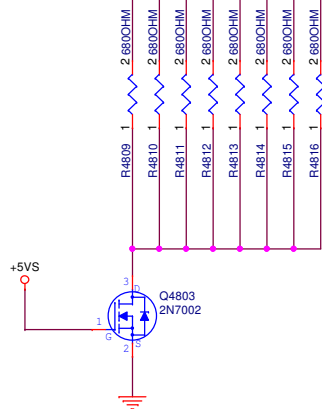


PEGATRON		Title : BUG_Debug	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size B	Project Name VGFTG		Rev 1.1
Date: Tuesday, December 11, 2012		Sheet 44 of 104	



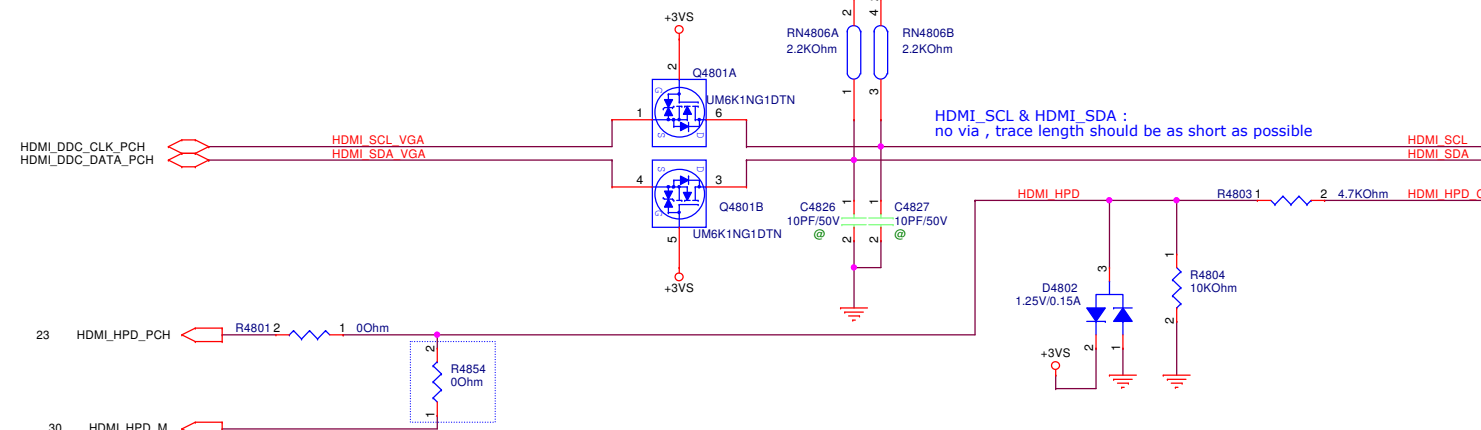
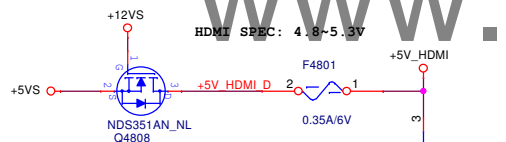
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23	HDMI_CLKP_PCH	C4809	1	2	0.1UF/25V	HDMI_CLKP
23	HDMI_CLKN_PCH	C4810	1	2	0.1UF/25V	HDMI_CLKN
23	HDMI_TXP0_PCH	C4811	1	2	0.1UF/25V	HDMI_TXP0
23	HDMI_TXN0_PCH	C4812	1	2	0.1UF/25V	HDMI_TXN0
23	HDMI_TXP1_PCH	C4813	1	2	0.1UF/25V	HDMI_TXP1
23	HDMI_TXN1_PCH	C4814	1	2	0.1UF/25V	HDMI_TXN1
23	HDMI_TXP2_PCH	C4815	1	2	0.1UF/25V	HDMI_TXP2
23	HDMI_TXN2_PCH	C4816	1	2	0.1UF/25V	HDMI_TXN2

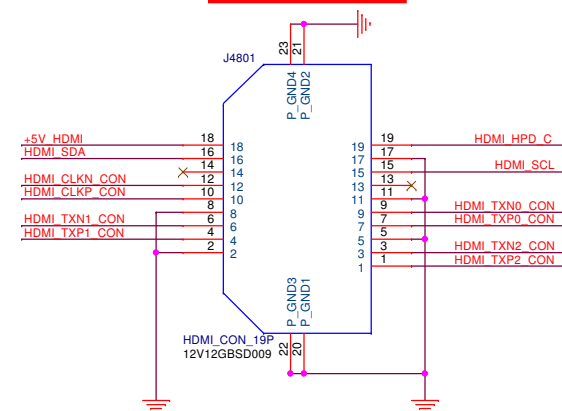


R1.1 For EMI change

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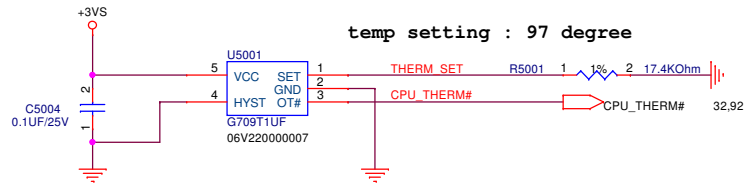


R1.1
M : 1212-00EU000

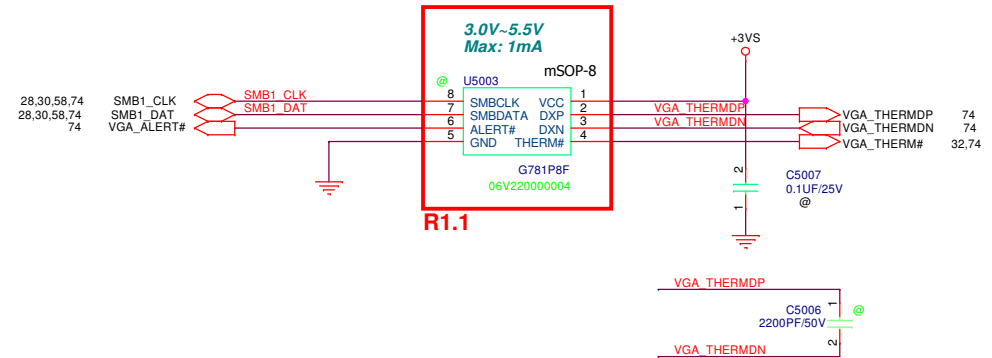


U5001 Close to CPU

temp setting : 97 degree



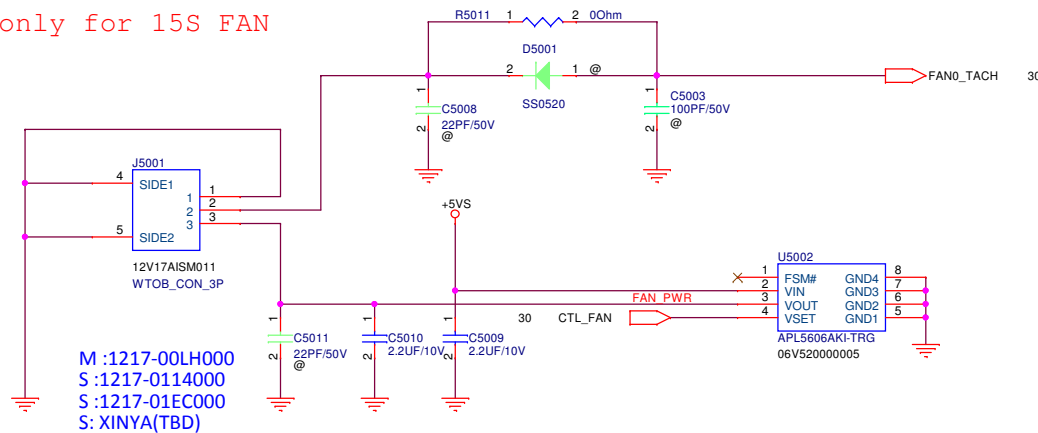
U5003 Close to GPU

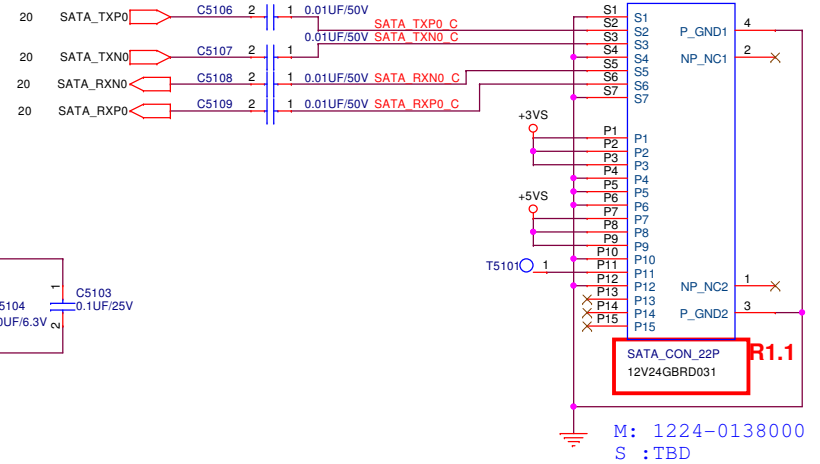
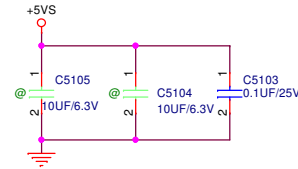
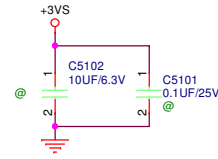


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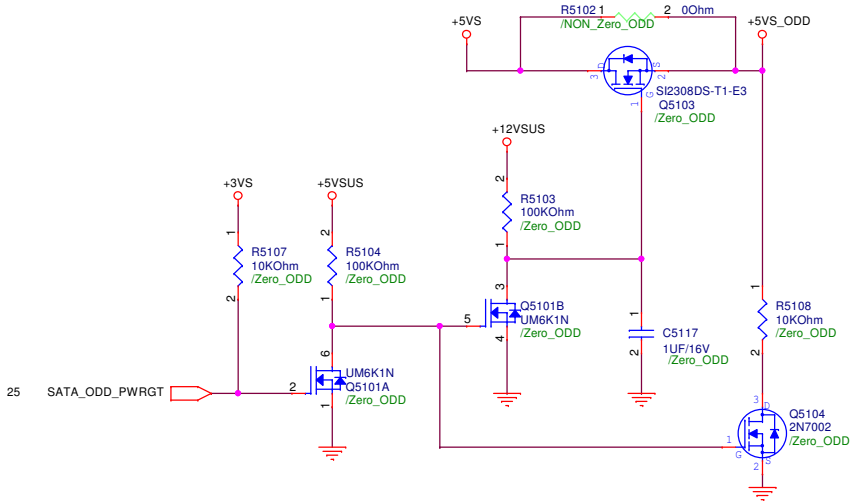
FAN

only for 15S FAN



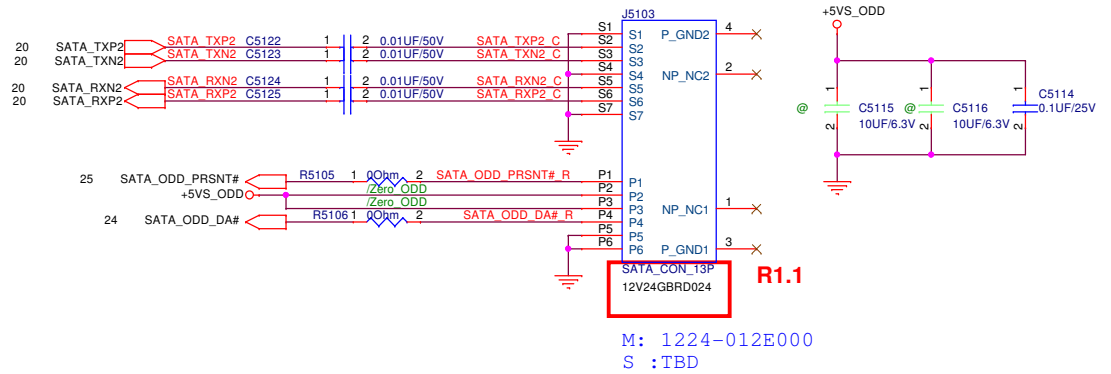


ZERO POWER ODD SUPPORT support Hokey turn off ODD power

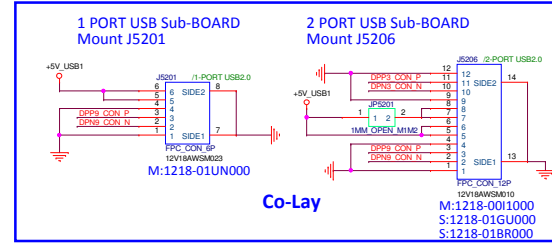
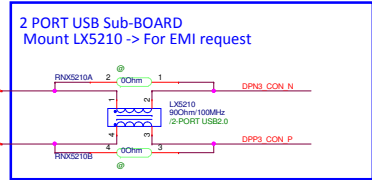
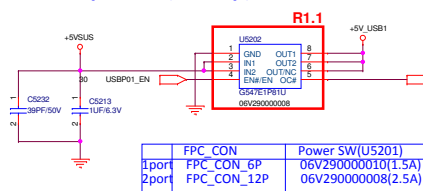


ODD Power Consumption MAX 1.8A /Cuntinue 1.1A

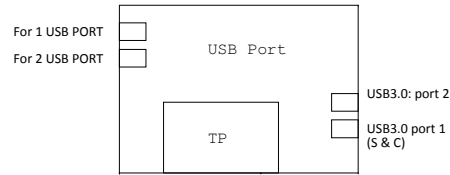
ODD



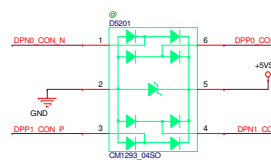
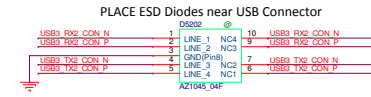
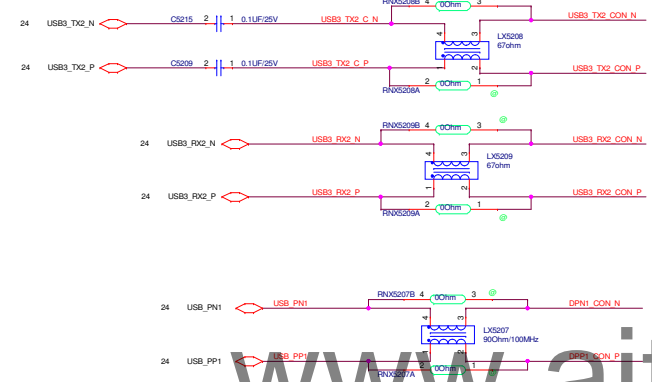
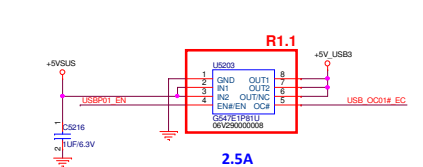
USB 2.0 port x2 (Left Up)



USB Sub-Board	Mount	Unmount
1port	J5201	J5206
2port	J5206	J5201



USB 3.0 ports x 1 without Sleep & Charge (Right Up)



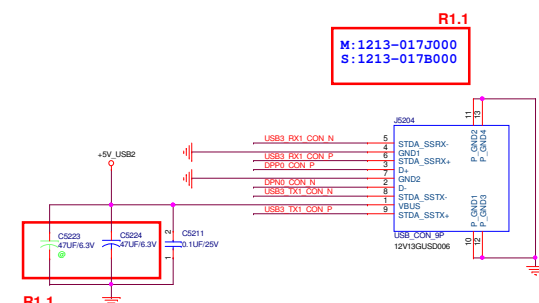
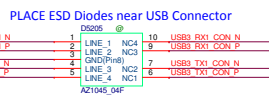
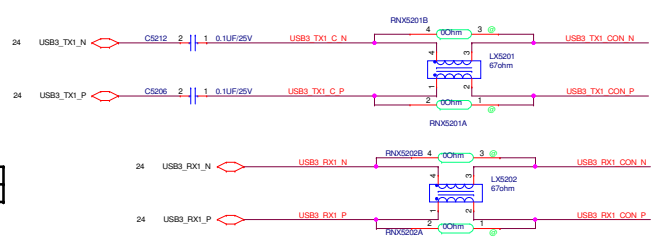
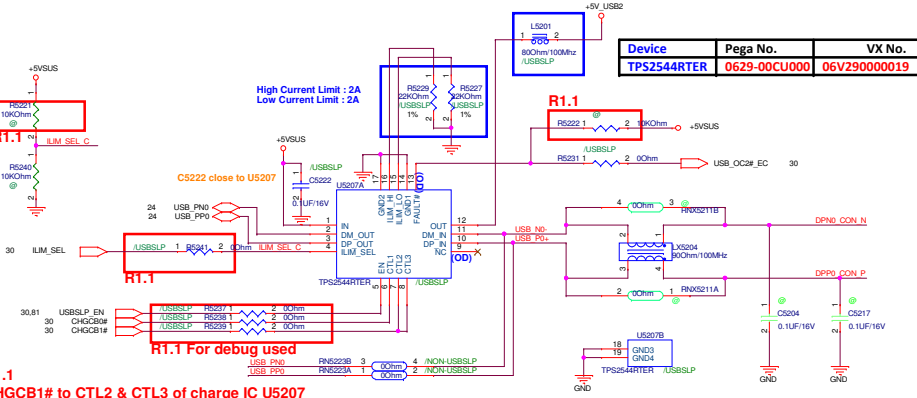
USBSLP / NON_USBSLP

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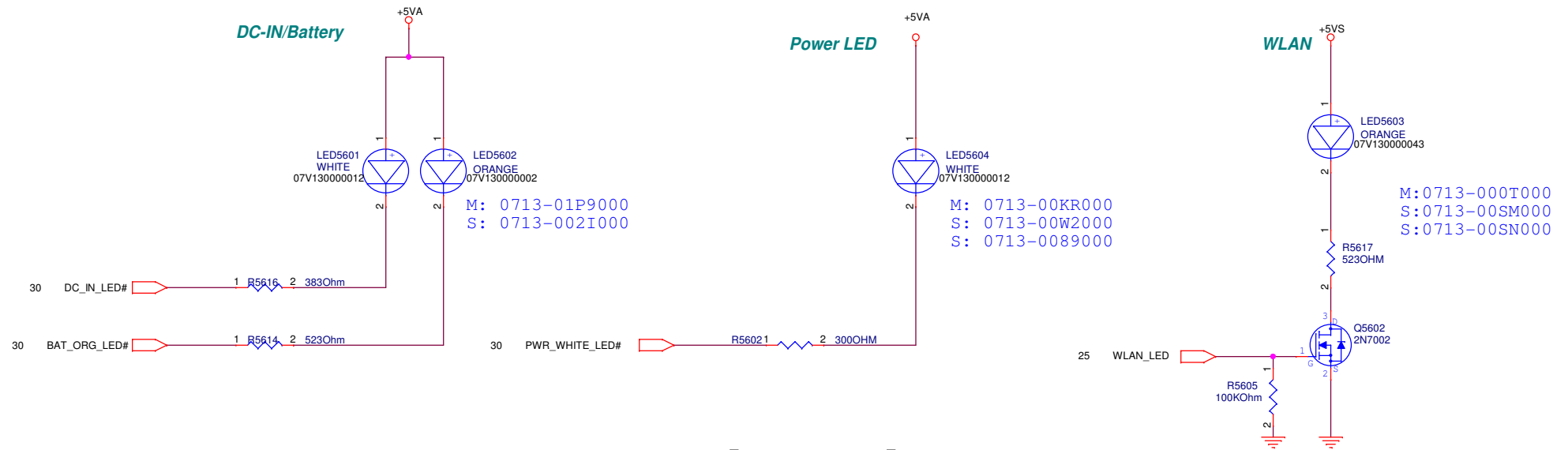
USB 3.0 ports x 1 with Sleep & Charge (Right Down)

TPS2544 Device True Table

Sleep & Charge function Setting	State	Charging Mode	Wake up	CHGCB0#	CHGCB1#	ILIM_SEL	USBSLP_EN	Backup
Auto Mode	S0	CDP	NA	1	1	1	1	Wake up by KB/MS at S3 state
	S3-S5	DCP Auto	NA	0	1	1	1	
Alternative Mode	S0	CDP	NA	1	1	1	1	Wake up by KB/MS at S3 state
	S3-S5	DCP Auto	NA	0	1	1	1	
Disable	S0	CDP	Enable wake up	1	1	0	1	Wake up by KB/MS at S3 state
	S3	SDP	Disable wake up	1	1	0	0	
	S4/S5	Discharge	NA	0	0	1	0	



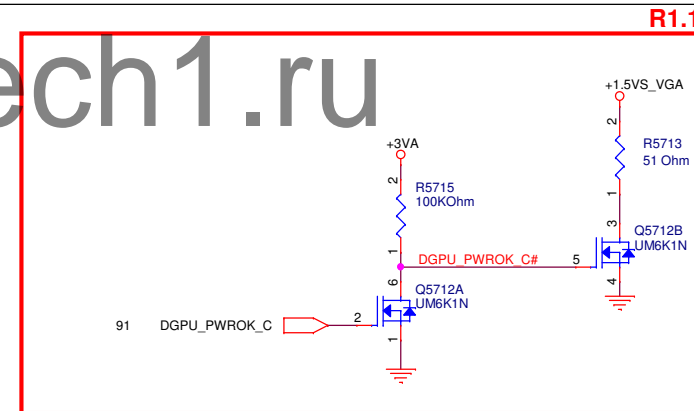
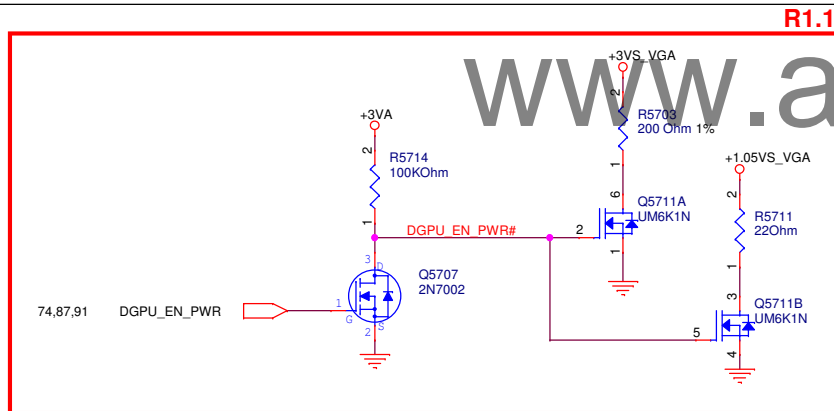
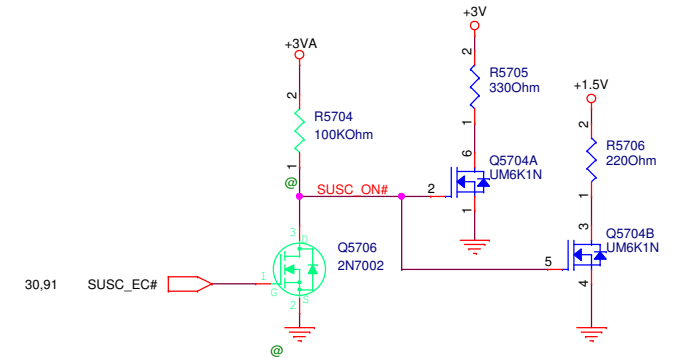
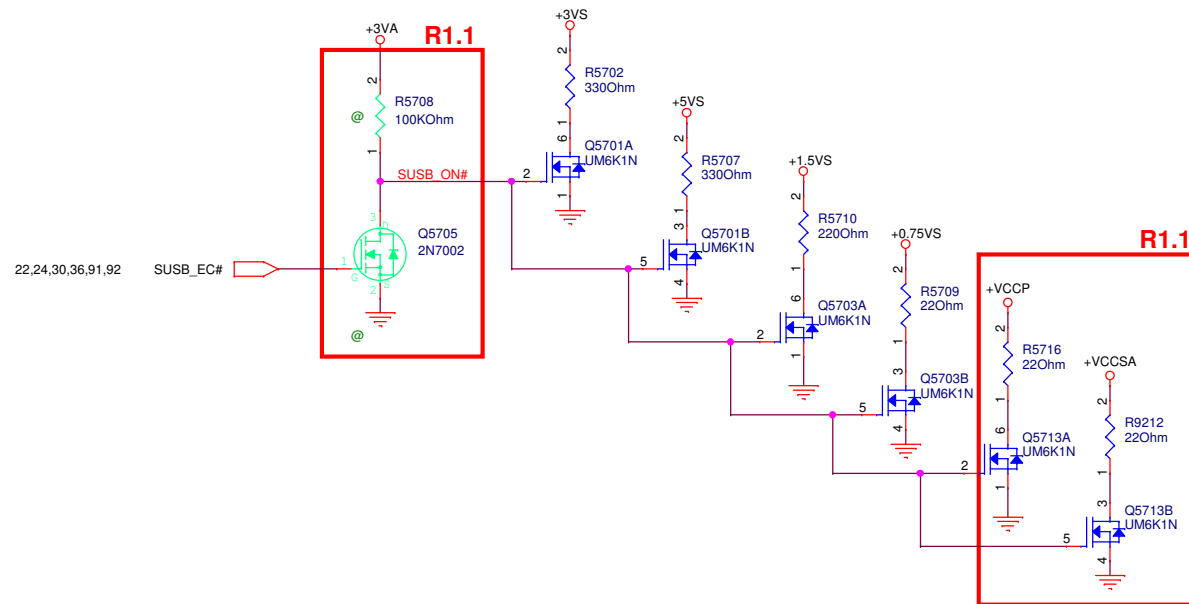
Order of Indicator LEDs



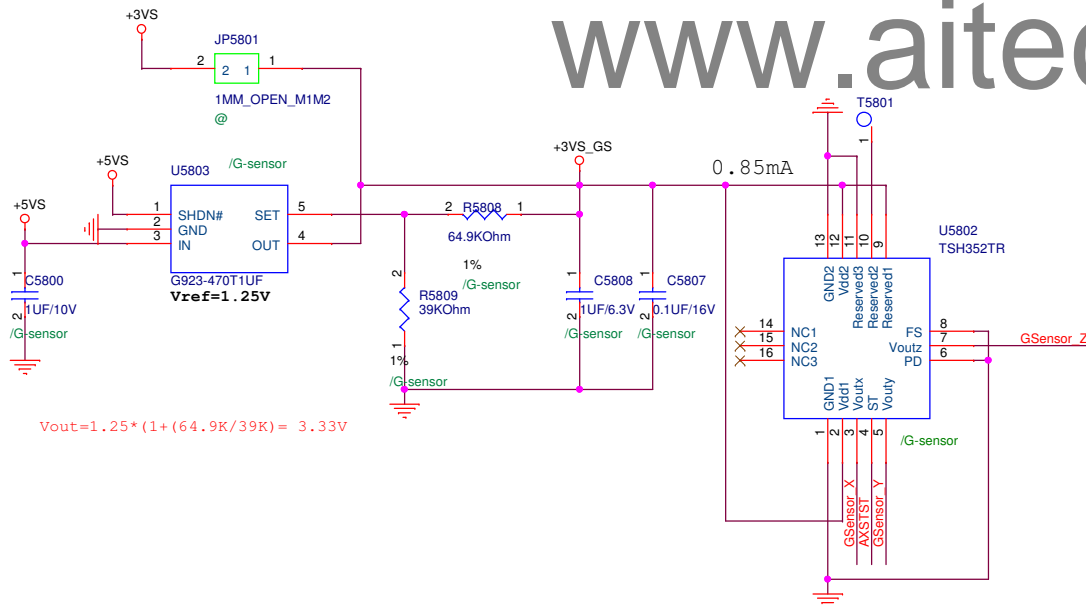
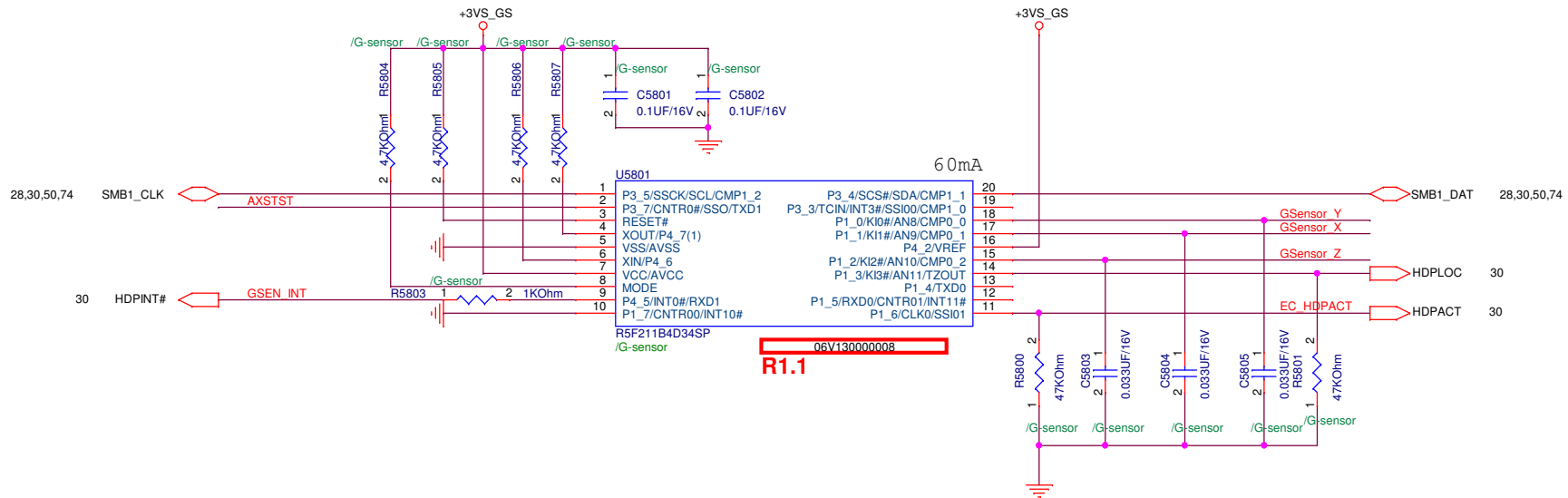
www.aitech1.ru

PEGATRON		Title : LED	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size B	Project Name VGFTG		Rev 1.1
Date: Tuesday, December 11, 2012		Sheet 56 of 104	

Discharge Circuit



G-sensor



$$V_{out} = 1.25 * (1 + (64.9K / 39K)) = 3.33V$$

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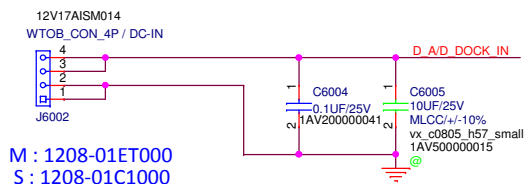
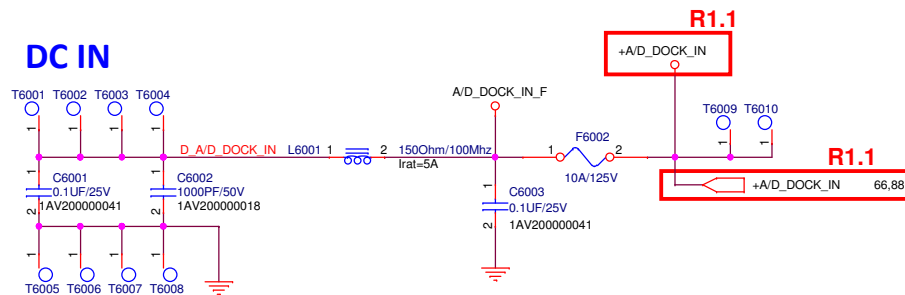
PEGATRON		Title : G-Sensor TSH35TR	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size B	Project Name		Rev 1.1
Date: Tuesday, December 11, 2012		Sheet 58	of 104

CIR

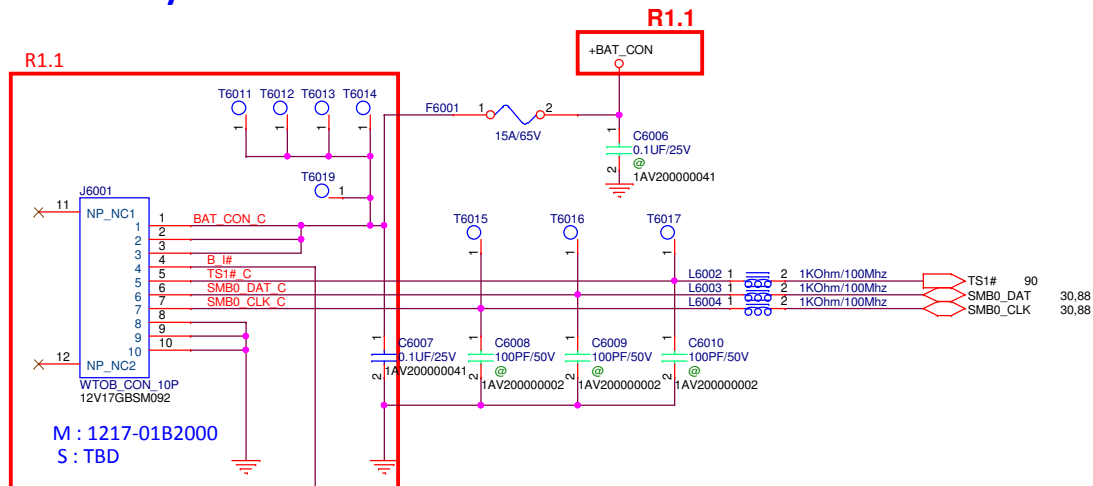
www.aitech1.ru

PEGATRON		Title :CIR	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size	Project Name		Rev
B			1.1
Date: Tuesday, December 11, 2012		Sheet	59 of 104

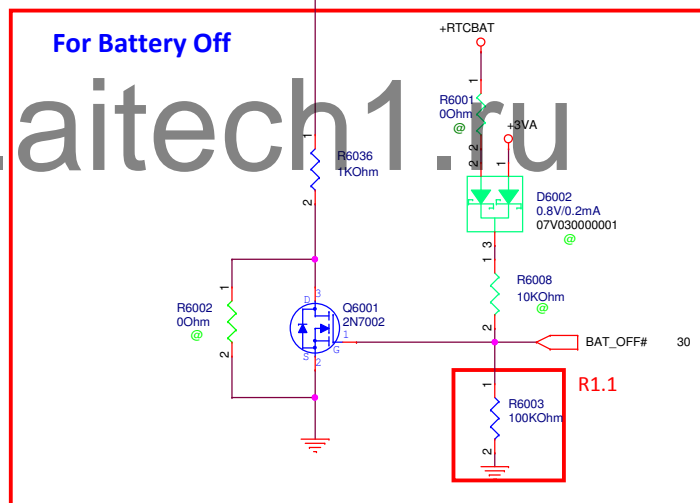
DC IN



Battery Connector



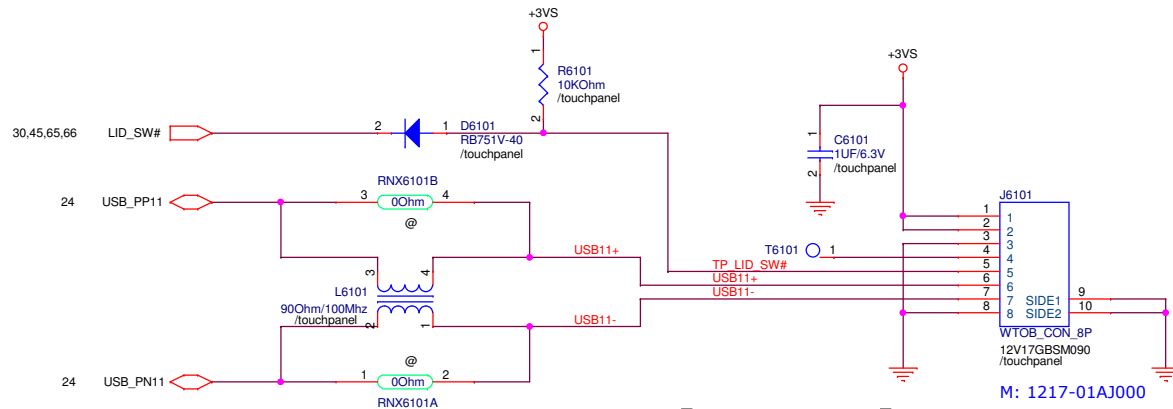
For Battery Off



PEGATRON		Title : DC-IN Battery	
BG1-CSC-HW R&D Dept.5		Engineer: Jim3_Liu	
Size	Project Name	Rev	
Custom	VGFTG	1.1	
Date: Tuesday, December 11, 2012		Sheet 60 of 104	

Touch Pad Module

R1.1 add LID_SW# at pin5



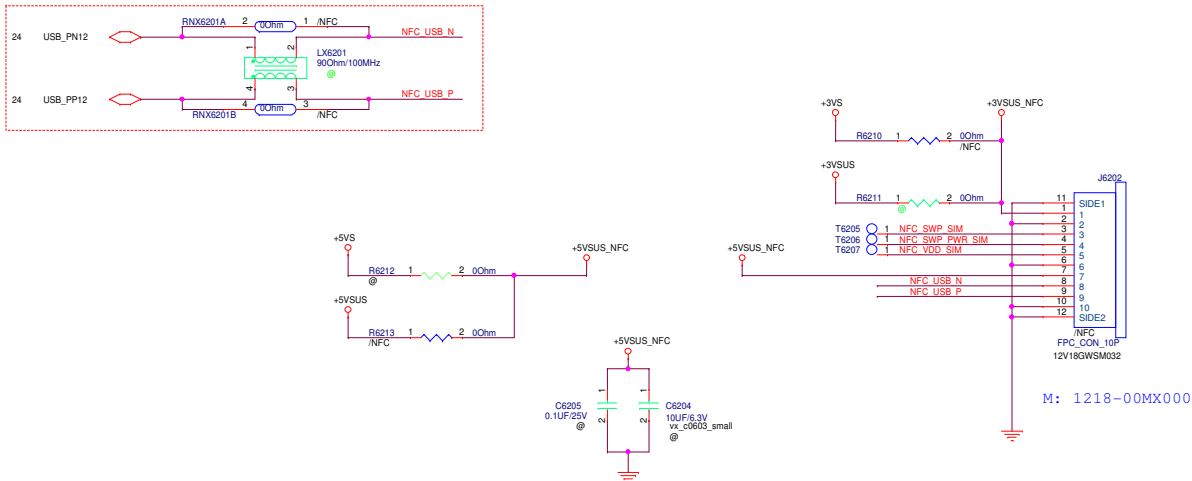
www.aitech1.ru

PEGATRON Title : Touch Panel		
BG1-CSC-HW R&D Dept.5		Engineer:
Size	Project Name	Rev
Custom		1.1
Date: Tuesday, December 11, 2012 Sheet 61 of 104		

www.aitech1.ru

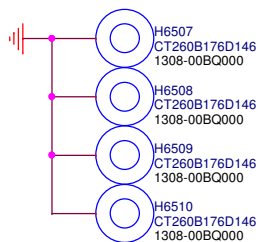
R1.1

NFC USB only for non Shark Bay platform

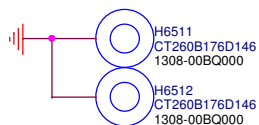


BGA

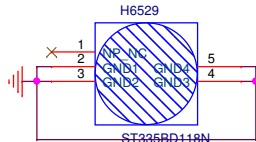
CPU NUTx4



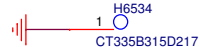
VGA NUTx2



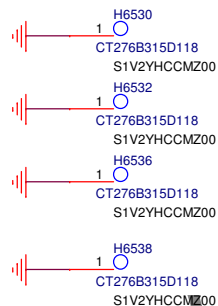
PCB : Screw A



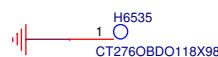
PCB : Screw B



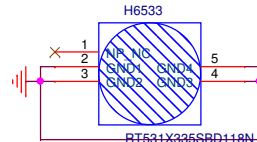
PCB : Screw Cx3



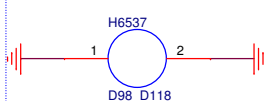
PCB : Screw D



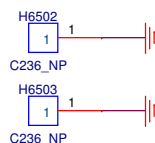
PCB : Screw F



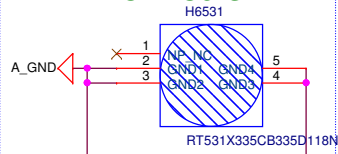
PCB : Screw G



GND PAD H*2

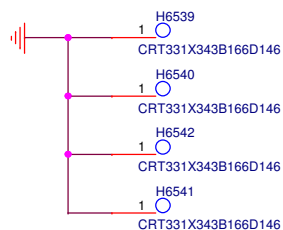


PCB : Screw E

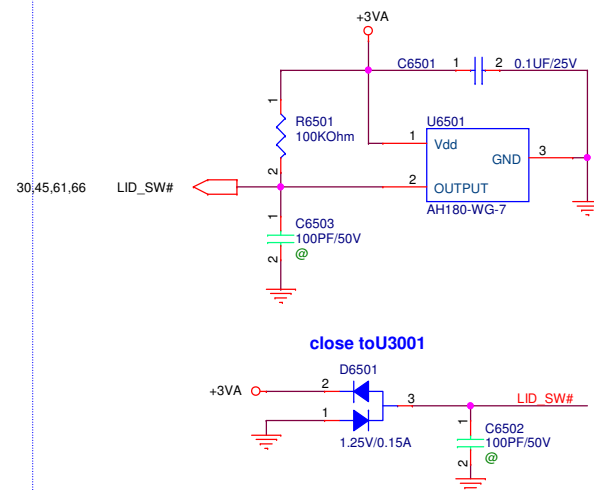


FTG STG

CPU PAD SCREWx4



LID Switch(Hall sensor)



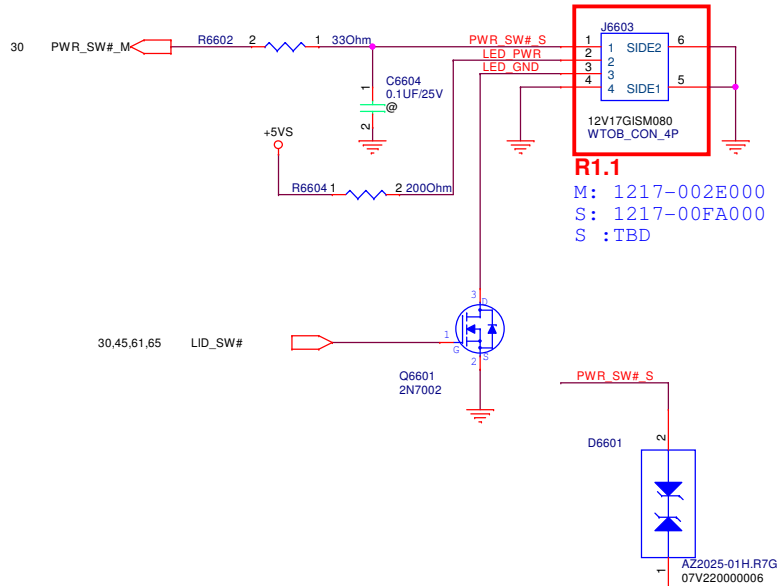
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

R1.1

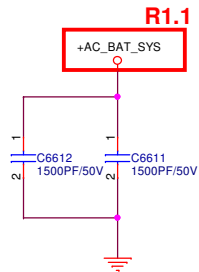
R1.1

PEGATRON		Title ME_CONN,Skew Hole	
Size B		Engineer: Jim3_Liu	
Project Name VGFTG		Rev 1.1	
Date: Tuesday, December 11, 2012		Sheet 65 of 104	

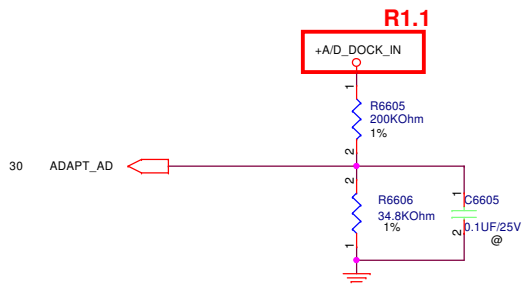
PWR BRD



EMI



ADAPTOR VOLTAGE DETECTOR.



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PCIEG => From CPU
PCIEG : to CPU

3 PCIEB_RXP[0..7]
3 PCIEB_RXN[0..7]

3 PCIEB_RXP[0..7]
3 PCIEB_RXN[0..7]

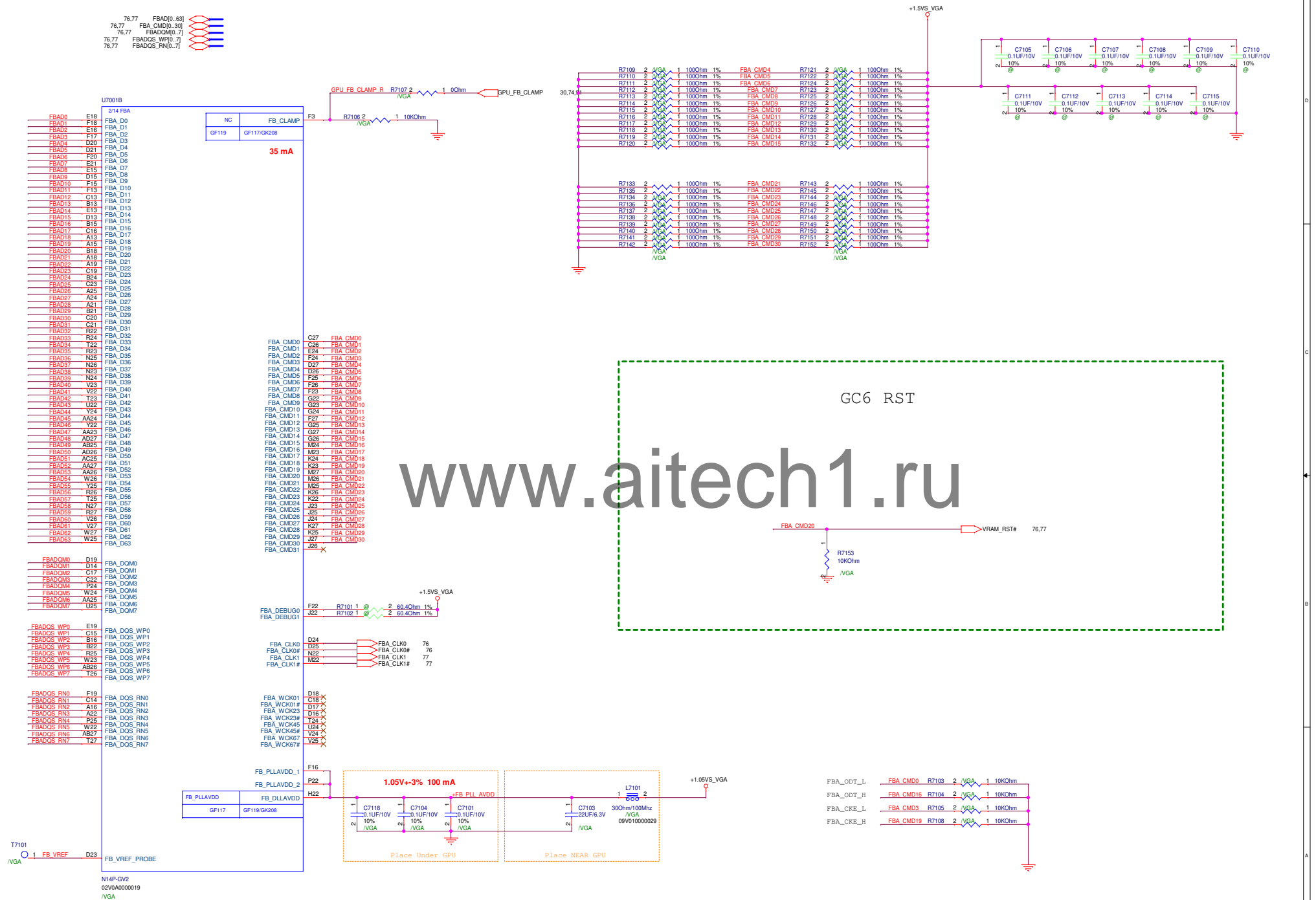
N14P-GV2
02V0A0000019
/VGA

PEGATRON Title :VGA-PCIE

BG1-CSC-HW R&D Dept.5 Engineer: Jim3 Liu

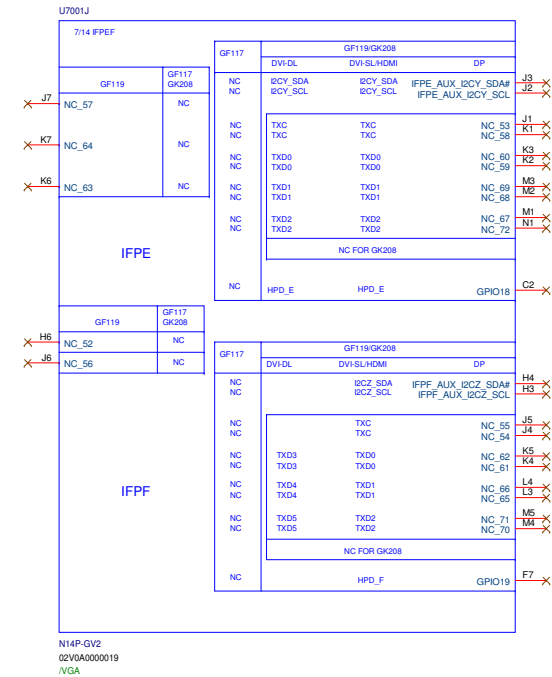
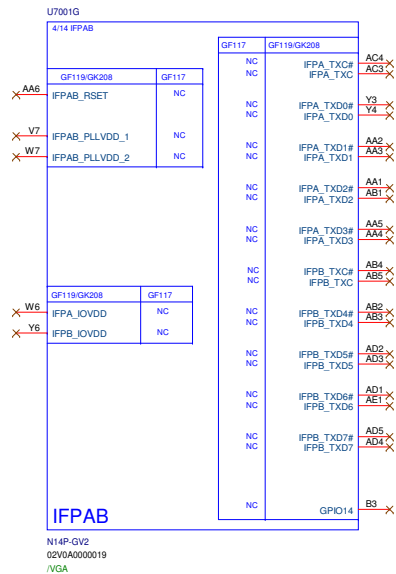
Size	Project Name	Rev
C	VGFTG	1.1
Date: Tuesday, December 11, 2012	Sheet 70 of 104	

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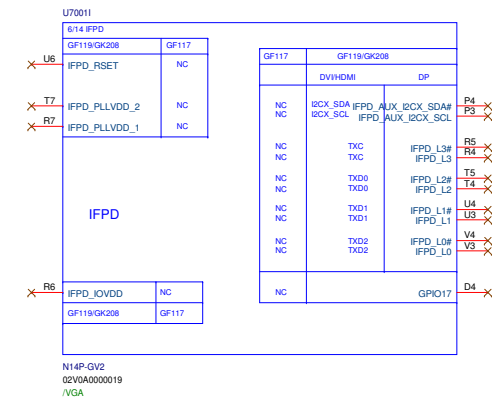
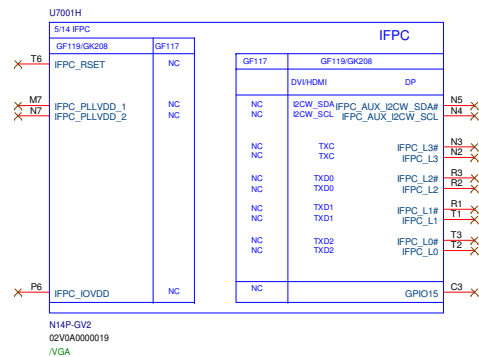


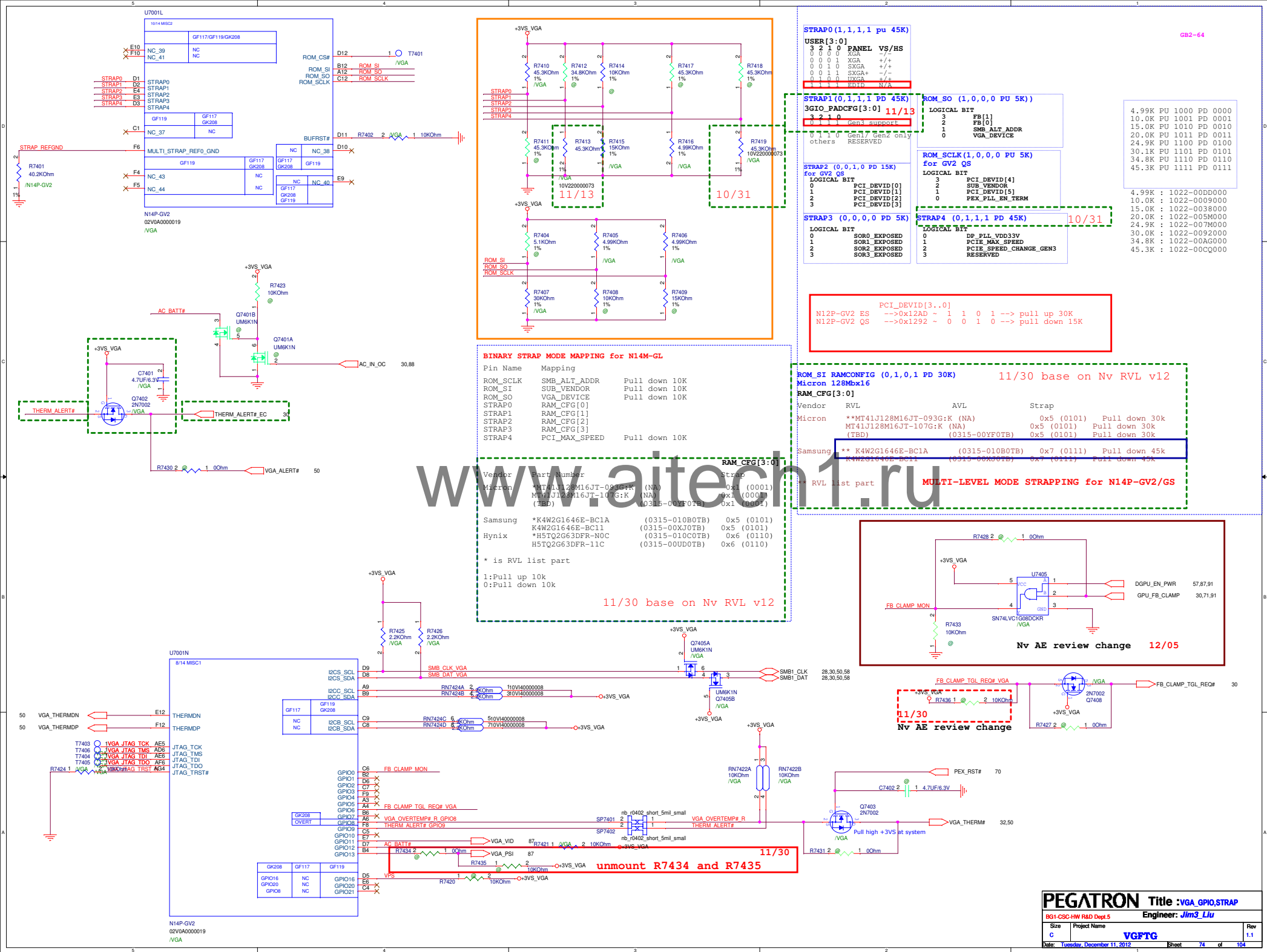
LVDS

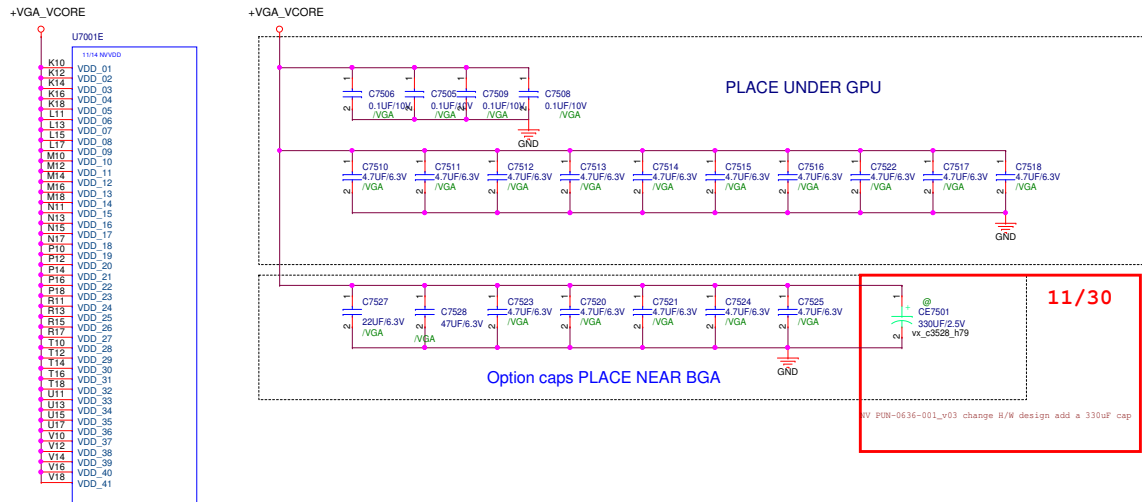


N14P-GV2
02V0A0000019
/VGA

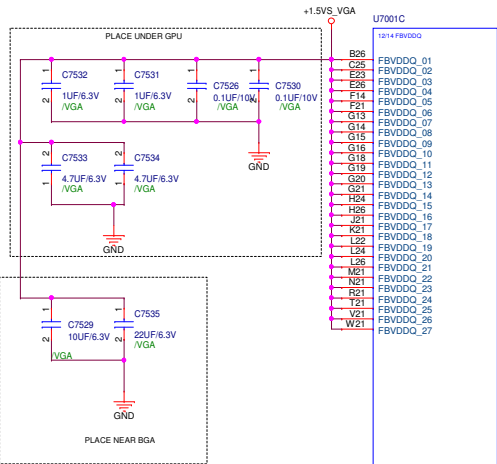
www.aitech1.ru



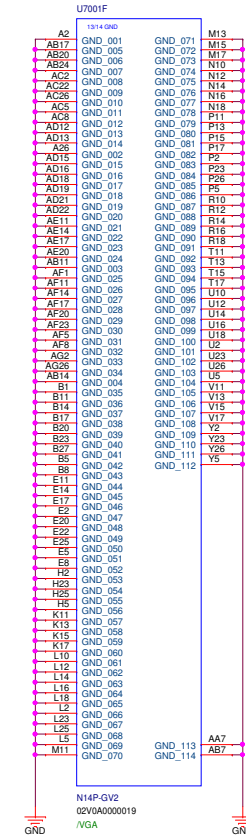
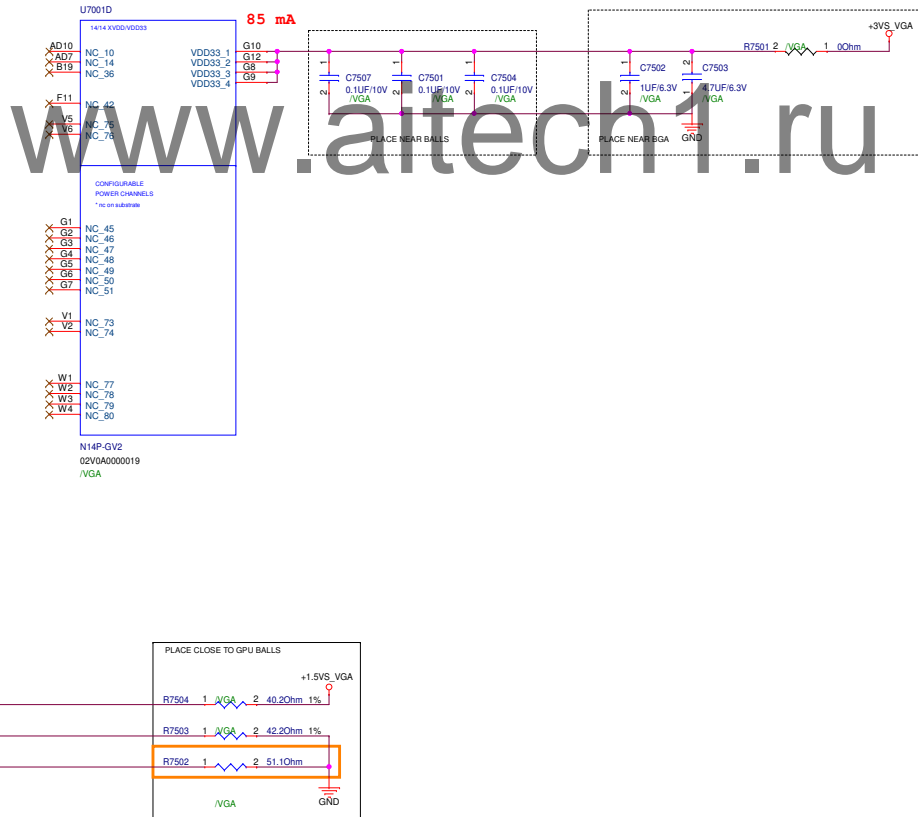




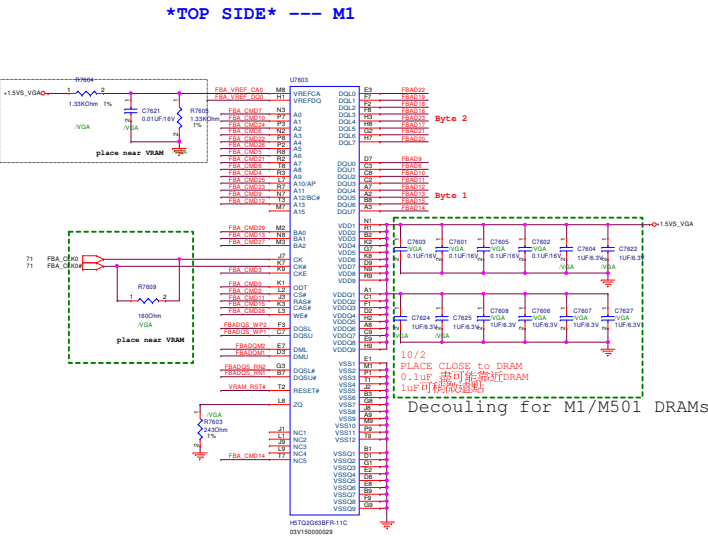
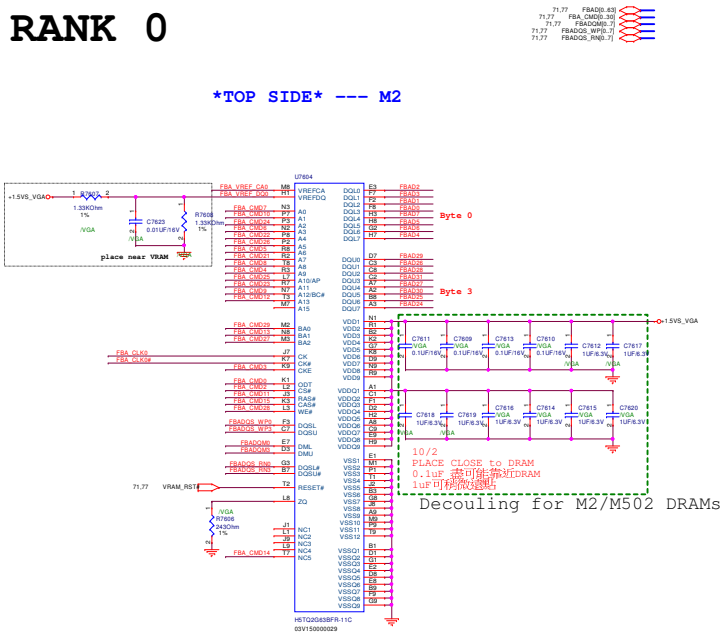
N14P-GV2
02V0A0000019
/VGA



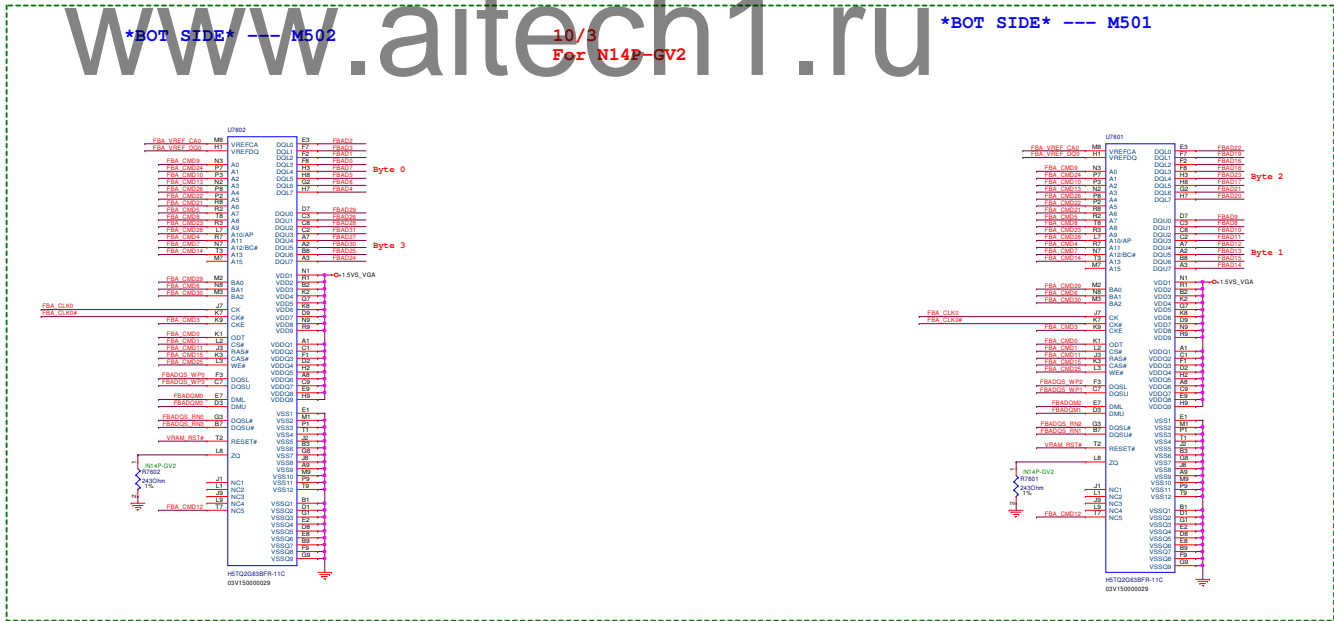
N14P-GV2
02V0A0000019
/VGA



FBA Partition 31..0 RANK 0

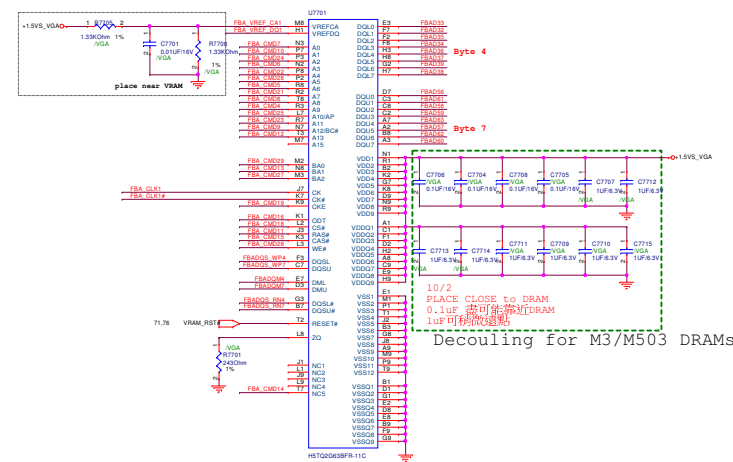
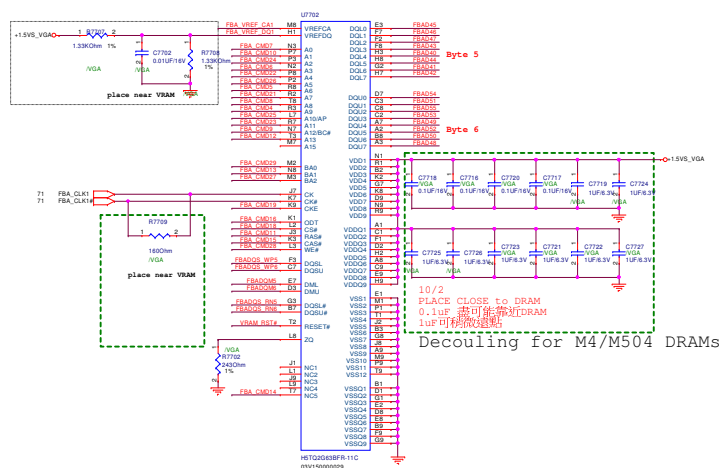


FBA Partition 31..0 RANK 1



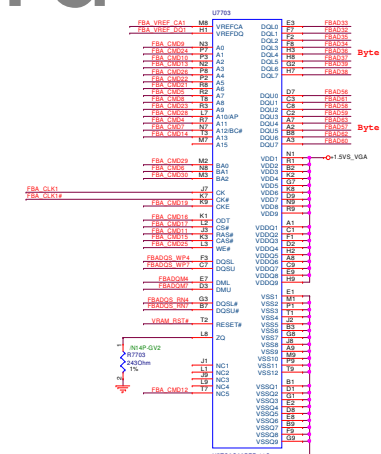
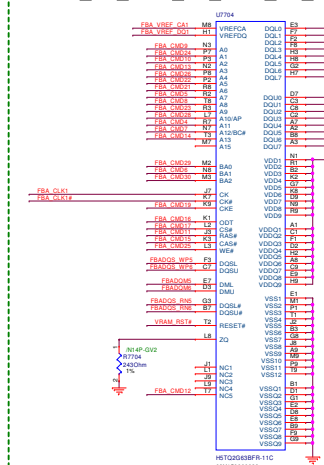
71,76	FBADQ[0.63]	
71,76	FBA_CMD[0.30]	
71,76	FBADQM[0.7]	
71,76	FBADQS_WP[0.7]	
71,76	FBADQS_RNO[0.7]	

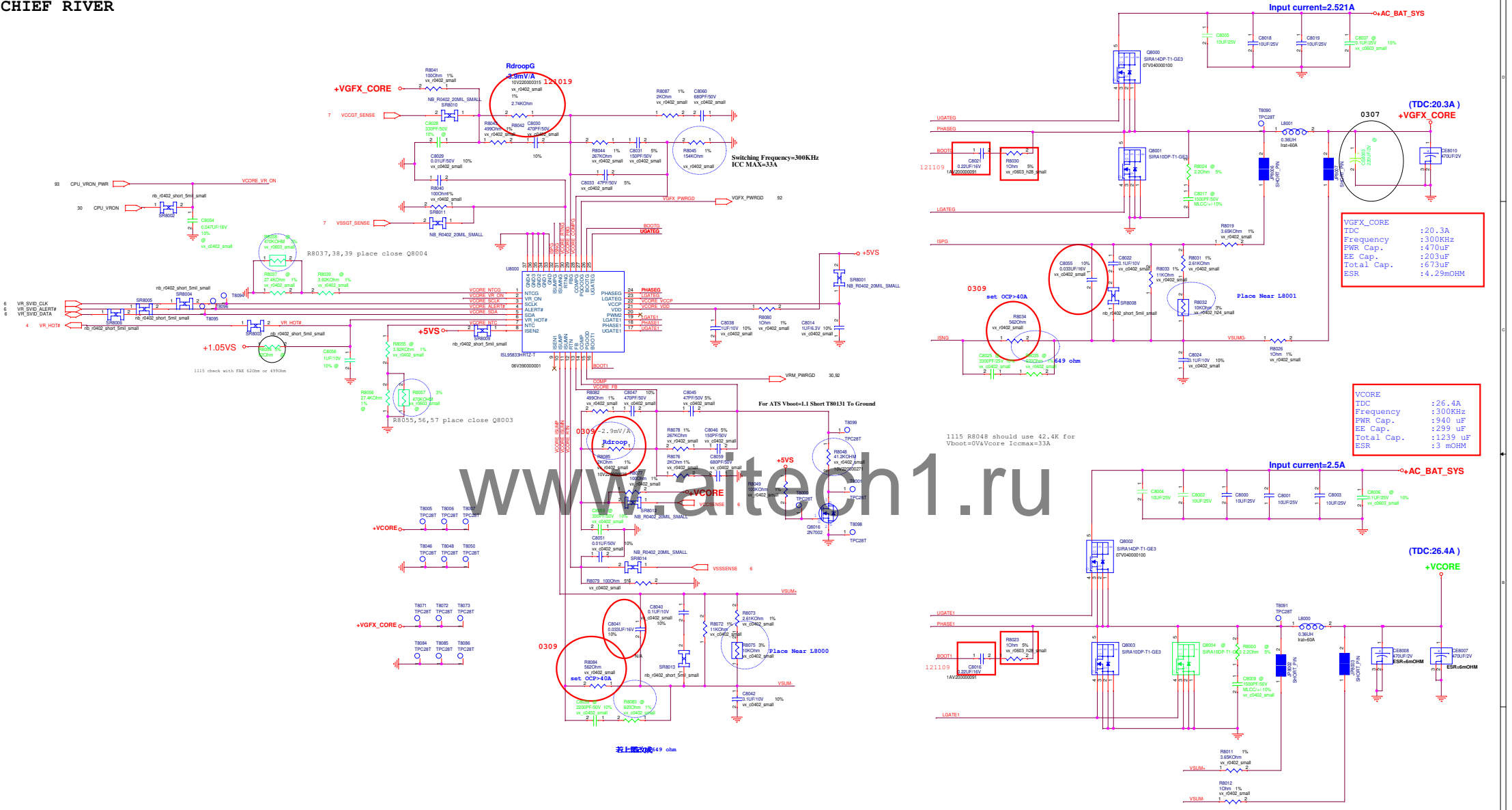
TOP SIDE --- M3



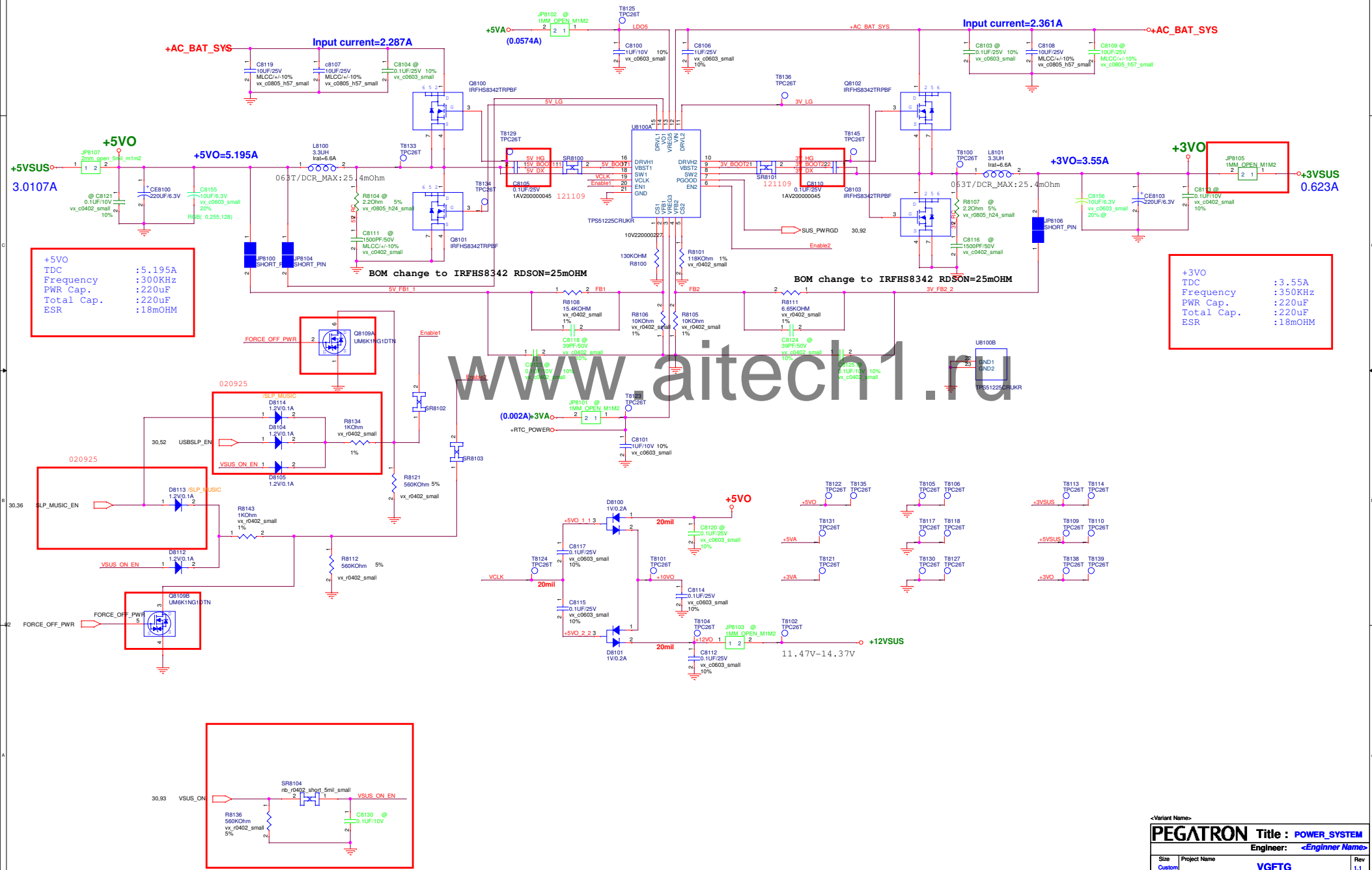
BOT SIDE --- M504 10/3
For N14P-GV2

BOT SIDE --- M503



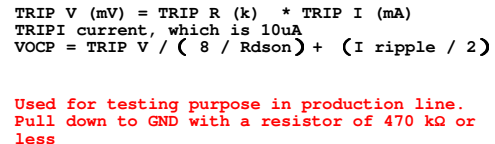


+5VO & +3VO POWER SUPPLY



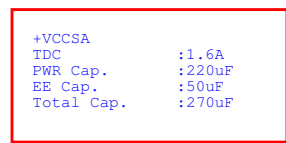
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IVB VCCSA POWER SUPPLY

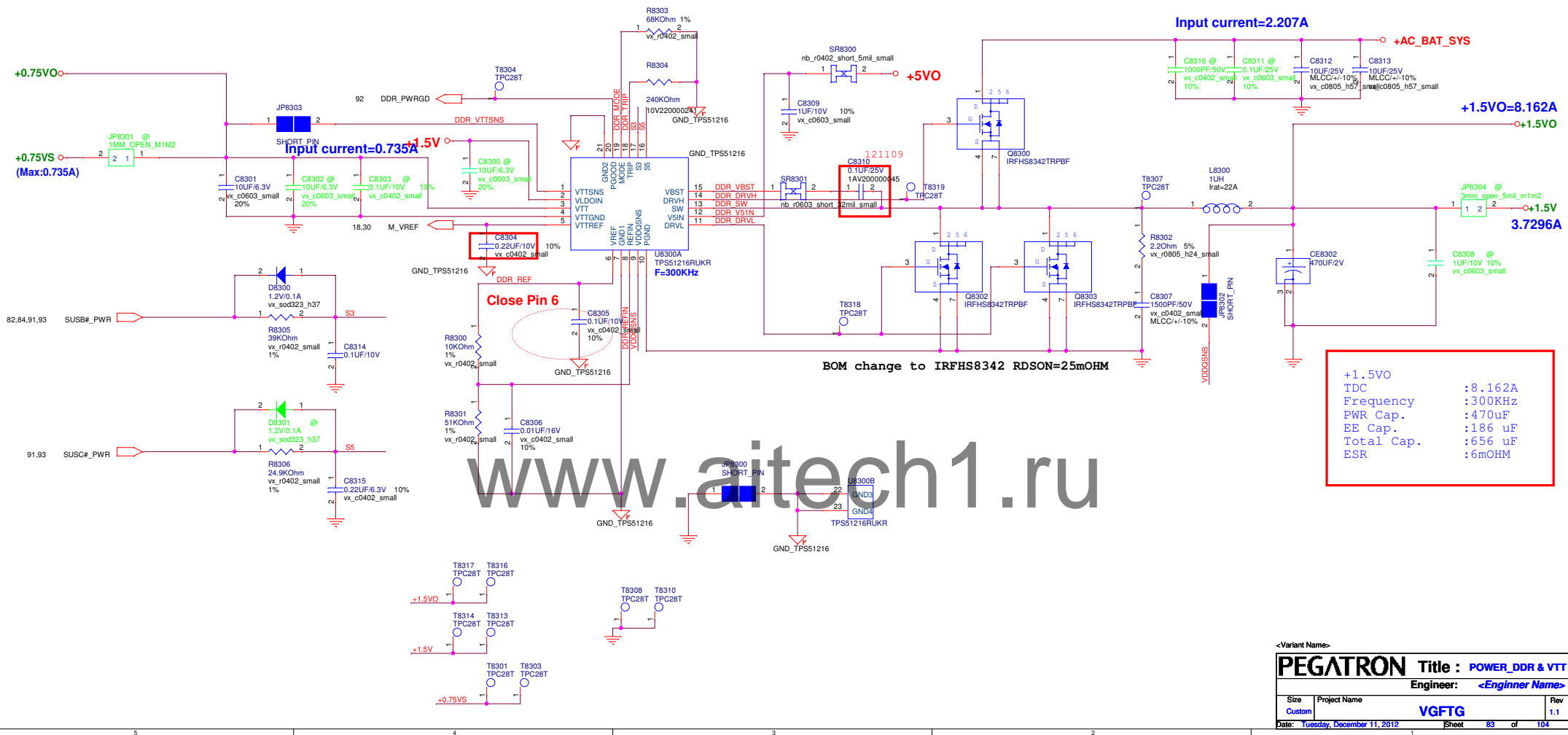


+1.05V0	
TDC	:8.6A
Frequency	:290KHz
PWR Cap.	:470uF
EE Cap.	:121 uF
Total Cap.	:591 uF
ESR	:9mOHM

+VCCSA_SELO	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V



DDR & VTT POWER SUPPLY

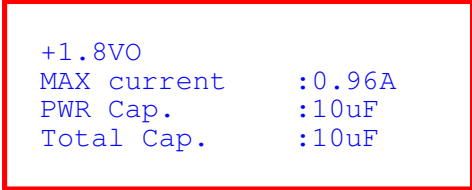


AV300000017

Vref=0.8V

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T8400 T8401 T8403
TPC26T TPC26T TPC26T



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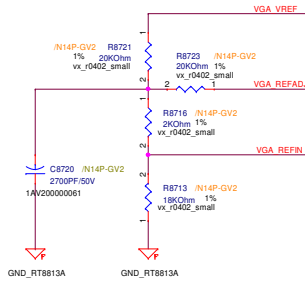
<Variant Name>		
PEGATRON Title : N/A		
Engineer:		
Size A4	Project Name	Rev 1.1
Date: Tuesday, December 11, 2012		Sheet 85 of 104

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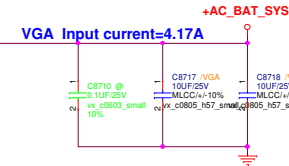
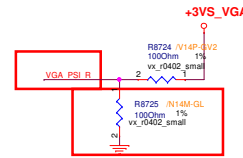
<Variant Name>

PEGATRON		Title : POWER_1.5VS	
Engineer: <i><Enginner Name></i>			
Size Custom	Project Name VGFTG		Rev 1.1
Date: Tuesday, December 11, 2012		Sheet 86 of 104	

VGA_CORE POWER SUPPLY



	one phase	two phase
R8723	39K	20K
R8721	30K	20K
R8716	3K	2K
R8713	27K	18K
C8703	>1.8nF	2.7nF
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.9V	0.9V
optional naming	/N14M-GL	/N14P-GV2

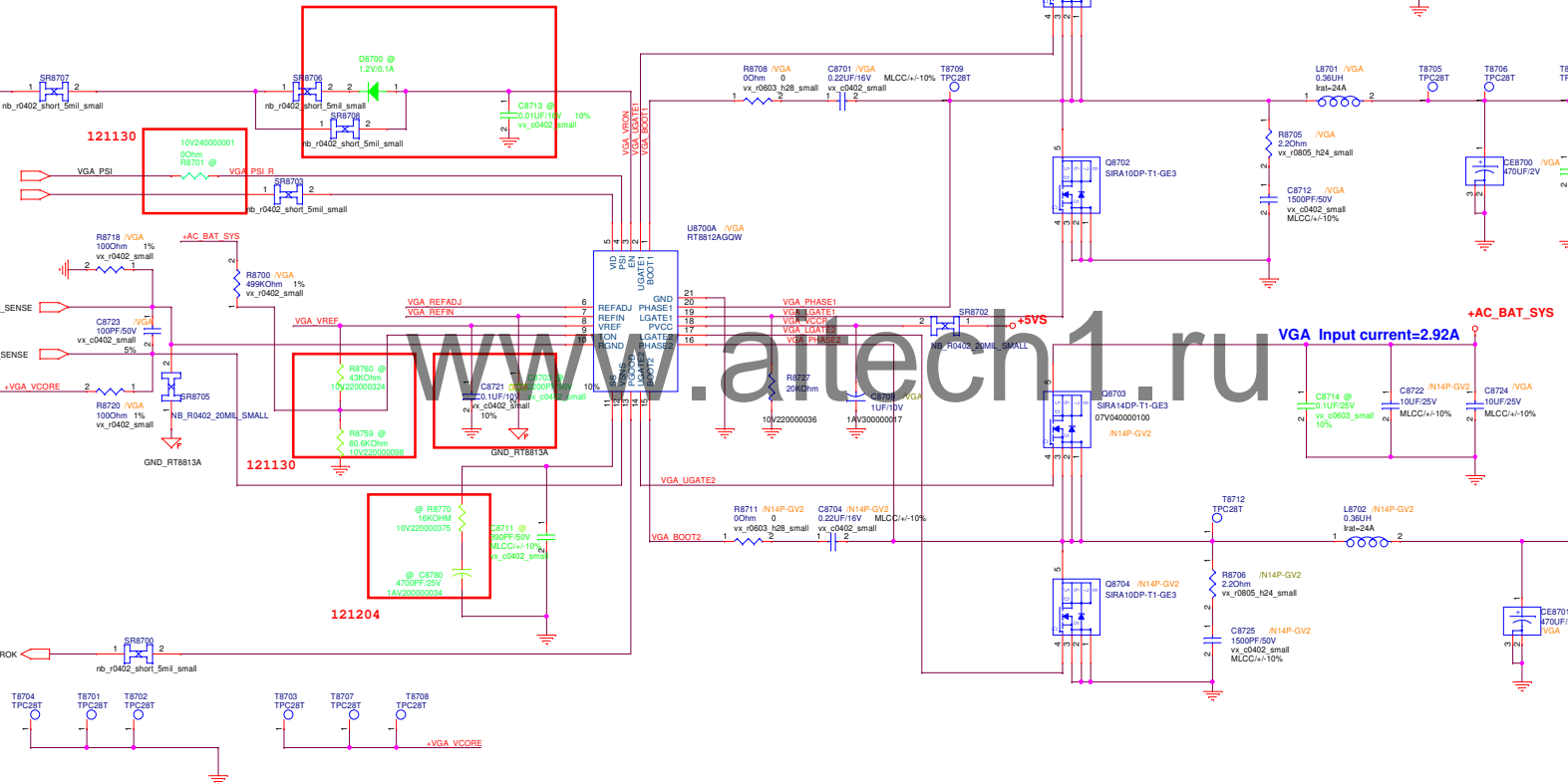
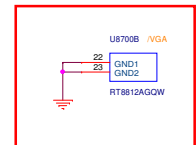


1 PHASE	2 PHASE
N14M-GL	N14P-GV2
EDP=20A	EDP=35A
TDC=20A	TDC=28A
OCP: 40A	OCP: 70A

+VGA_VCORE (2 Phase)	
TDC	:28A
Frequency	:305KHz
PWR Cap.	:940uF
EE Cap.	:139.5uF
Total Cap.	:1079.5uF
ESR	:3mOHM

+VGA_VCORE (1 Phase)	
TDC	:20A
Frequency	:305KHz
PWR Cap.	:940uF
EE Cap.	:139.5uF
Total Cap.	:1079.5uF
ESR	:3mOHM

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM



<Variant Name>

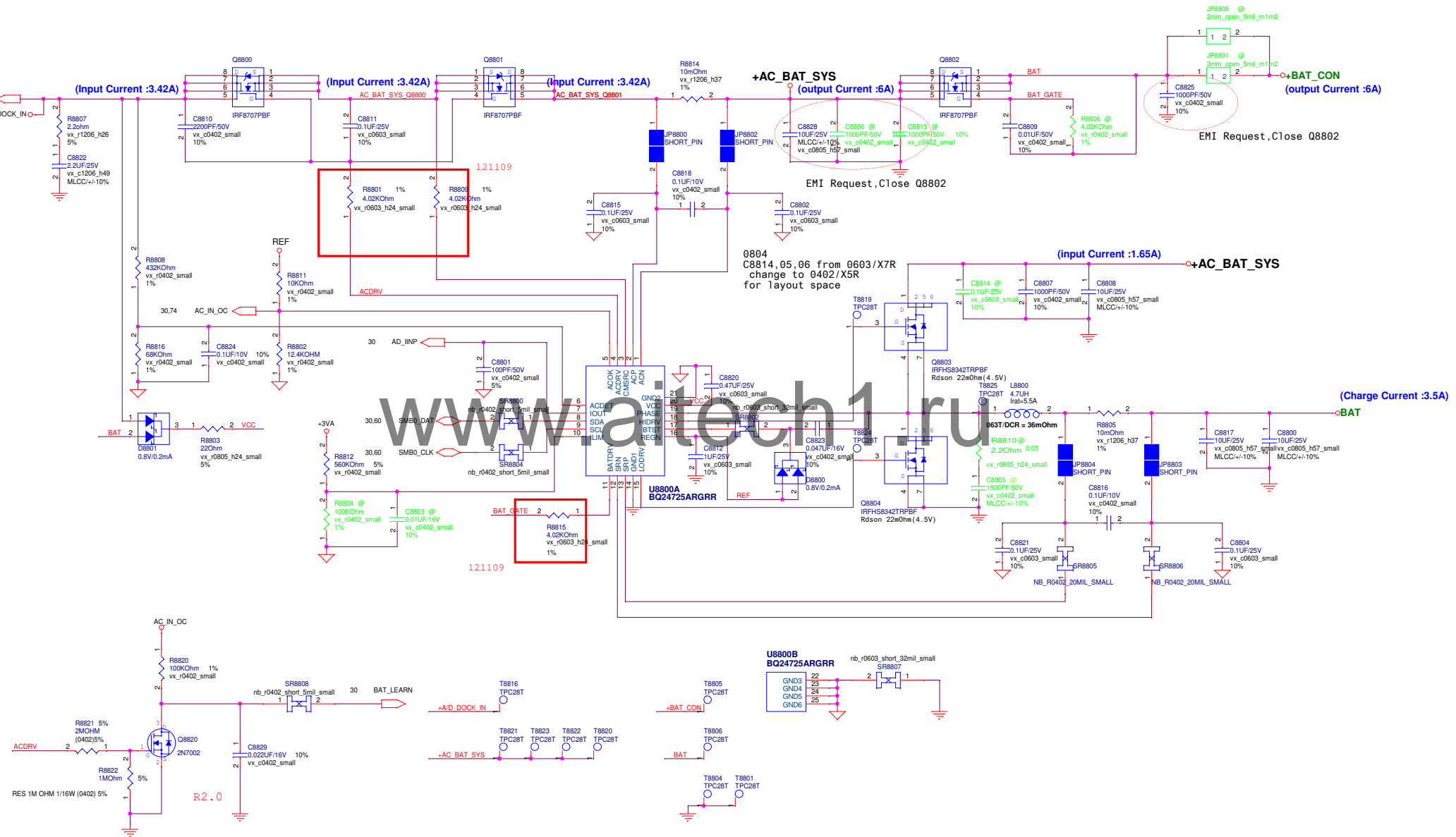
PEGATRON Title : POWER_VGACORE

Engineer: <Engineer Name>

Size Project Name
Custom VGF7G Rev 1.1

Date: Tuesday, December 11, 2012 Sheet 87 of 104

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

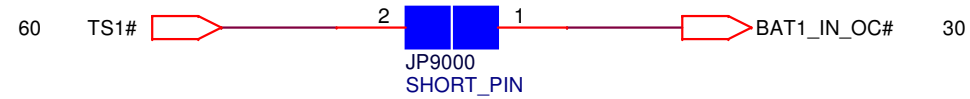
Engineer: <i><Enginner Name></i>		
Size Custom	Project Name VGFTG	Rev 1.1
Date: Tuesday, December 11, 2012	Sheet 88 of 104	

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<Variant Name>

PEGATRON		Title :	POWER_N/A	
		Engineer:	<Enginner Name>	
Size Custom	Project Name VGFTG			Rev 1.1
Date: Tuesday, December 11, 2012		Sheet	89	of 104

BATTERY IN DETECT

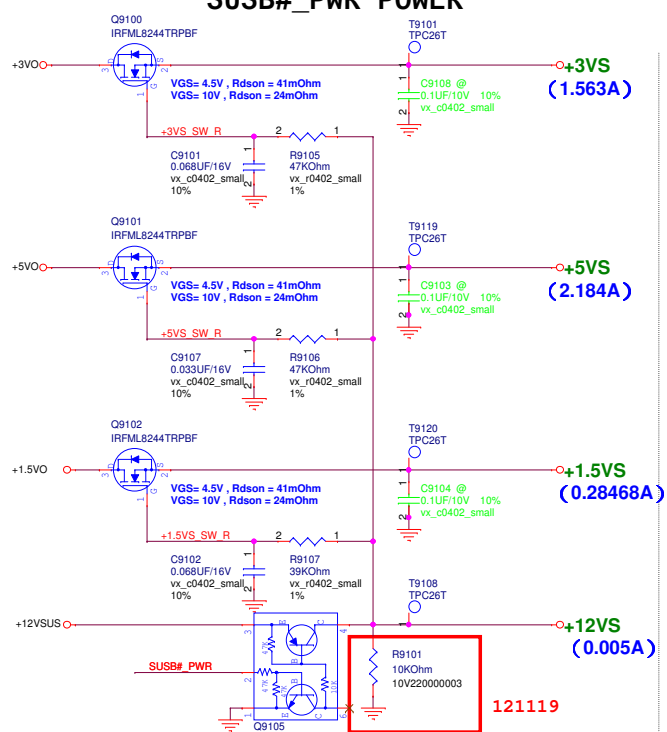


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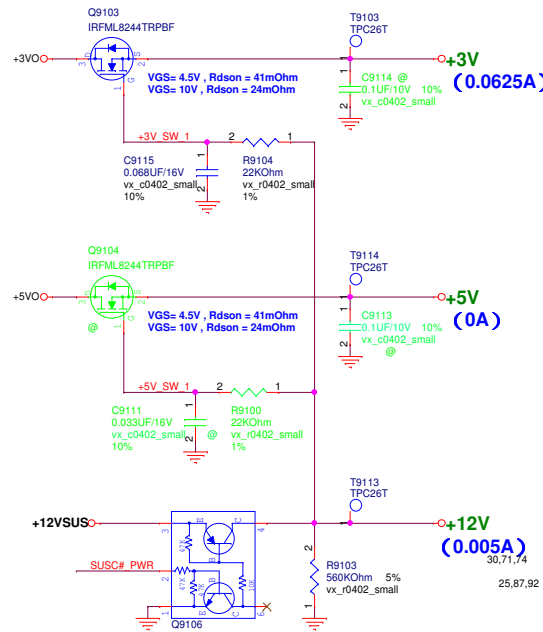
<Variant Name>

PEGATRON		Title : POWER_DETECT	
		Engineer: <Enginner Name>	
Size Custom	Project Name VGFTG		Rev 1.1
Date: Tuesday, December 11, 2012		Sheet	90 of 104

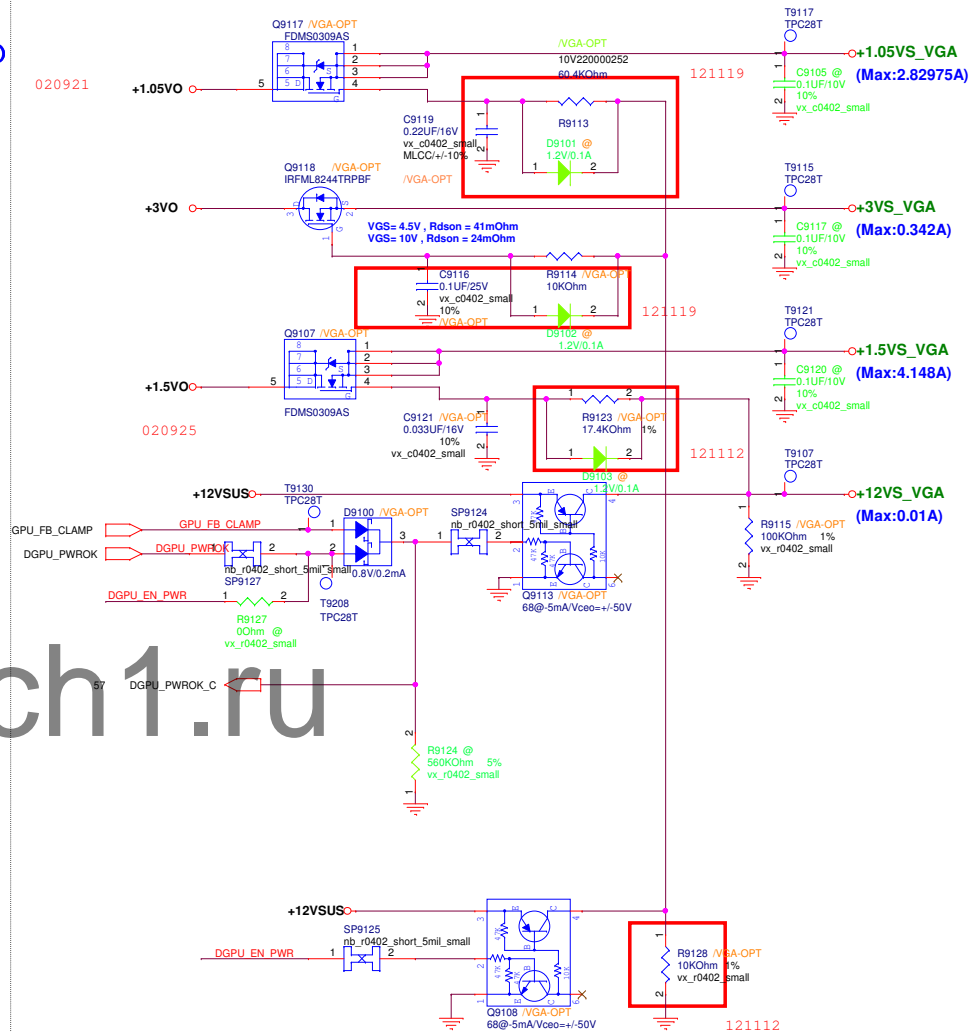
SUSB#_PWR POWER



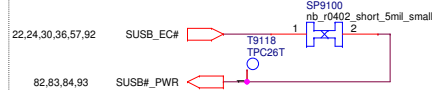
SUSC#_PWR POWER



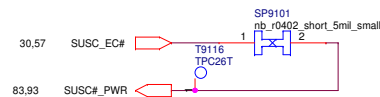
DSC#_PWR POWER(DGPU)



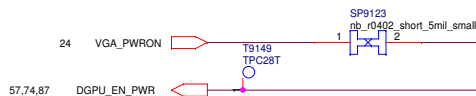
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



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<Variant Name>

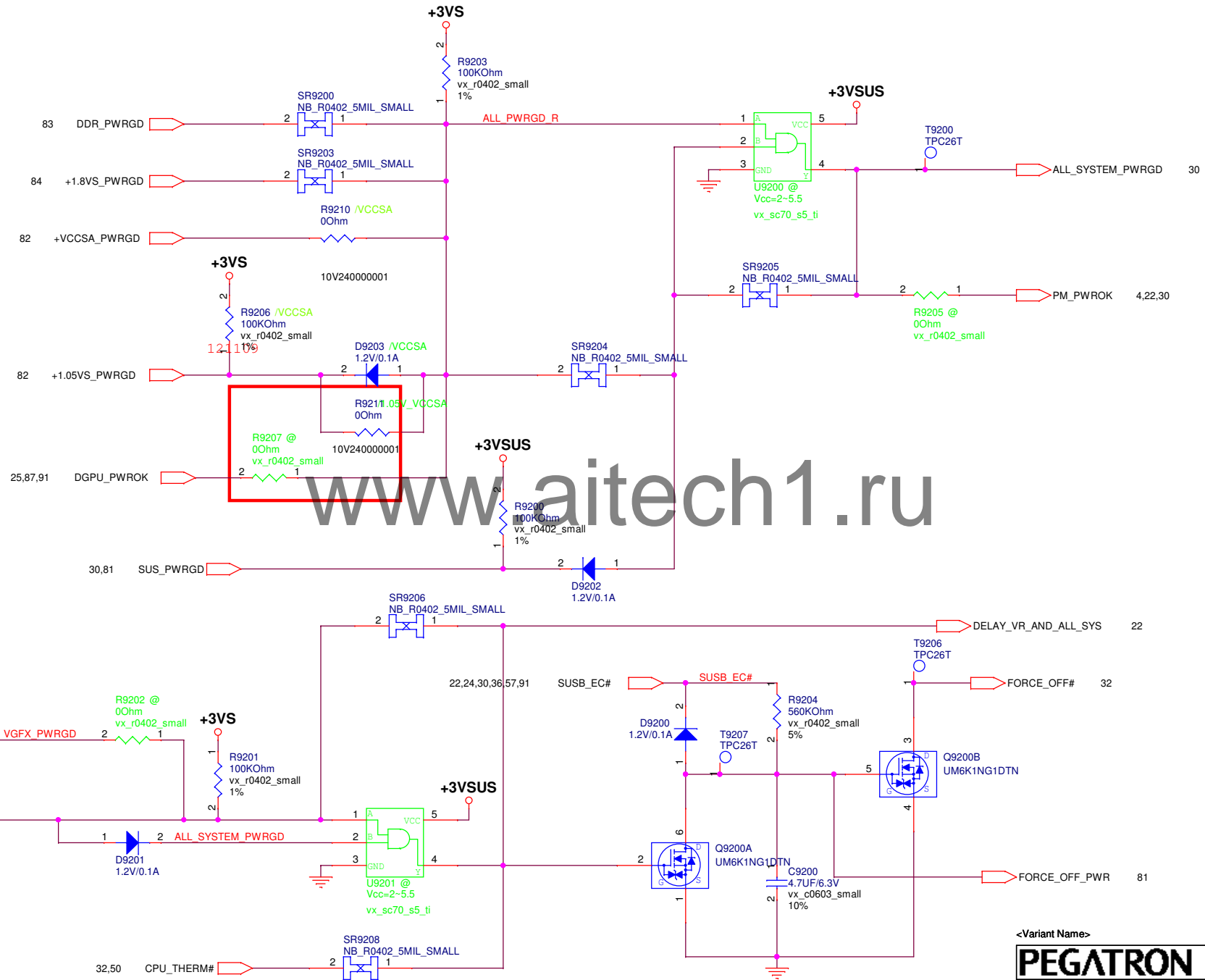
PEGATRON Title :POWER_LOAD SWITCH

Engineer: <Enginner Name>

Size Project Name VGFITG

Date: Tuesday, December 11, 2012 Sheet 91 of 104

POWER GOOD DETECTOR

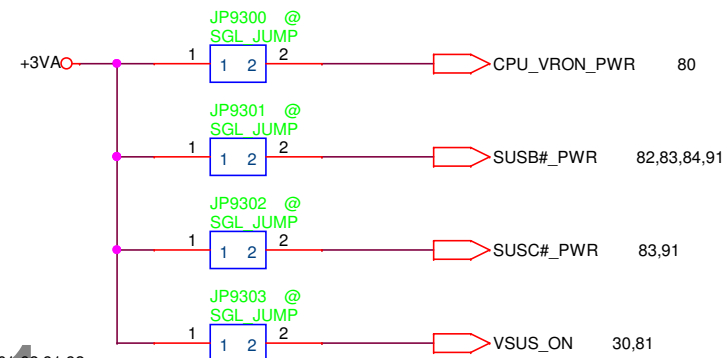


<Variant Name>

PEGATRON		Title : POWER_PROTECT	
Size		Engineer: <Engineer Name>	
Custom	Project Name	VGFTG	
Date: Tuesday, December 11, 2012	Sheet 92	of 104	
Rev 1.1			

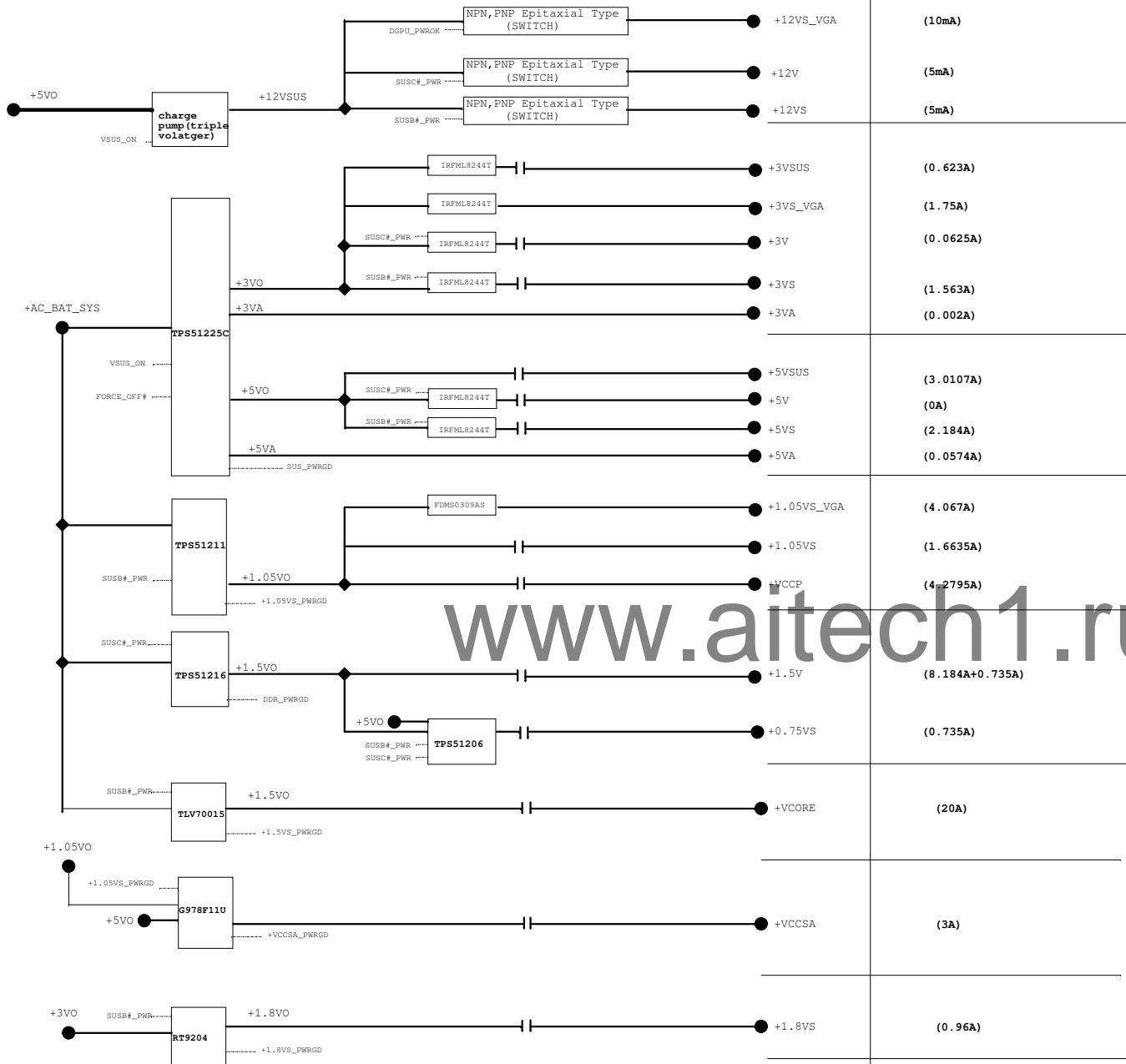
+AC_BAT_SYS	+AC_BAT_SYS	45,66,80,81,82,83,87,88
+BAT_BAT	BAT_88	
+BAT_CON	+BAT_CON	60,88
+5VA	+5VA	56,81
+3VA	+3VA	6,20,30,33,37,57,60,65,81,88
+5VO	+5VO	36,81,82,83,84,91
+3VO	+3VO	36,70,81,84,91
+1.8VO	+1.8VO	84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	22,33,36,51,81,91
+5VSUS	+5VSUS	22,27,51,52,62,81,82
+3VSUS	+3VSUS	22,24,27,28,30,33,34,37,53,62,81,92
+12V	+12V	91
+5V	+5V	91
+3V	+3V	24,44,45,57,91
+12VS	+12VS	28,31,48,91
+5VS	+5VS	20,27,30,31,36,37,46,48,50,51,56,57,58,62,66,80,87,91
+3VS	+3VS	3,4,16,17,20,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+1.8VS	+1.8VS	7,25,26,84
+1.5VS	+1.5VS	26,53,57,91
+VCCP	+VCCP	3,4,6,7,26,27,32,57,82
+1.05VS	+1.05VS	26,27,80,82
+VCCSA	+VCCSA	7,57,82
+0.75VS	+0.75VS	16,17,57,83
+12VS_VGA	+12VS_VGA	91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+VGA_VCORE	+VGA_VCORE	75,87

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: <Enginner Name>	
Size	Project Name		Rev
Custom	VGFTG		1.1
Date: Tuesday, December 11, 2012		Sheet	93 of 104



SPEC rating
(10mA)
(5mA)
(5mA)
(0.623A)
(1.75A)
(0.0625A)
(1.563A)
(0.002A)
(3.0107A)
(0A)
(2.184A)
(0.0574A)
(4.067A)
(1.6635A)
(4.2795A)
(8.184A+0.735A)
(0.735A)
(20A)
(3A)
(0.96A)

<Variant Name>

PEGATRON

Title : POWER_FLOWCHART

Engineer: <Engineer Name>

Rev

Project Name

Customer

VGFTG

Rev

1.1

Date

10/20/2013

Sheet

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of

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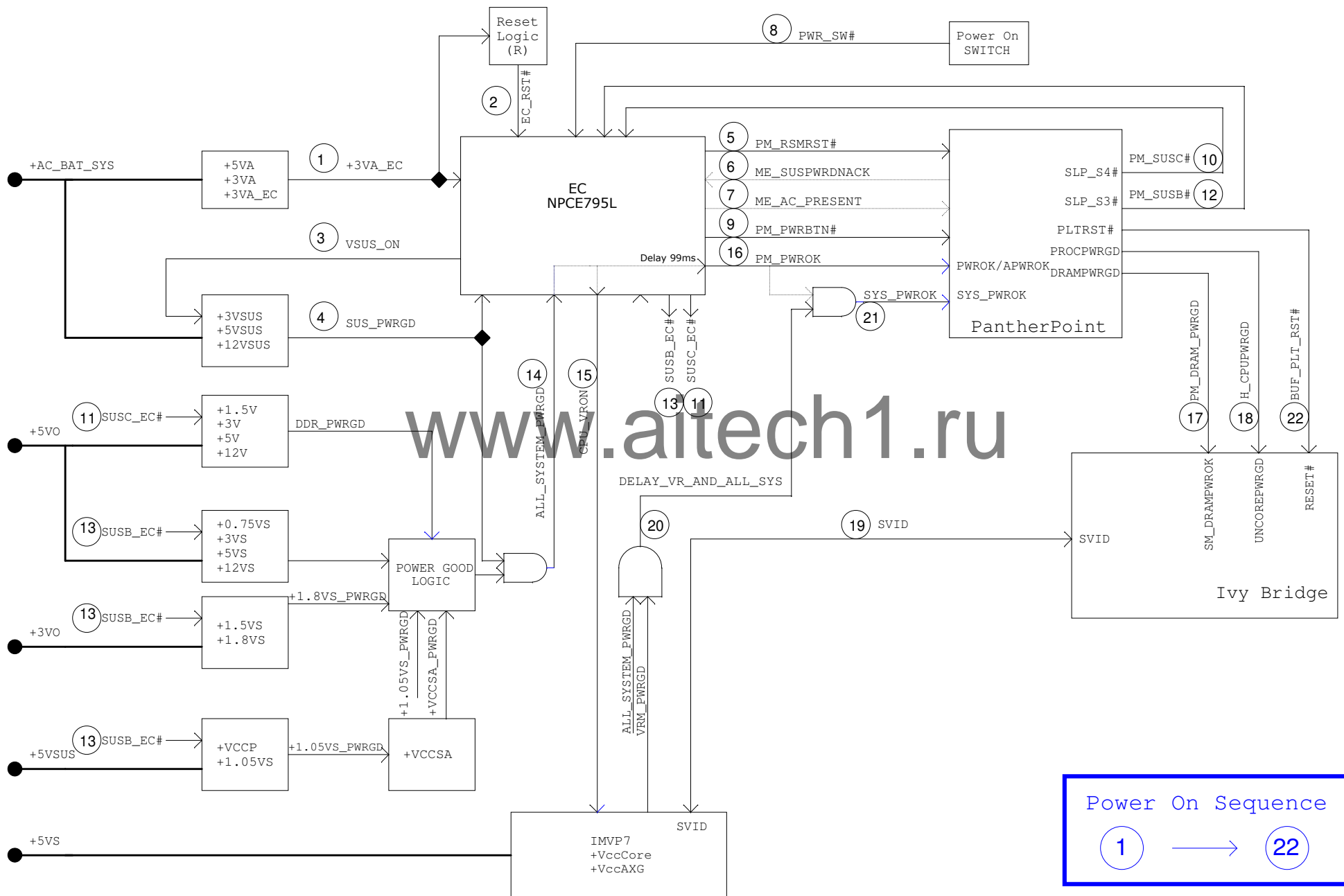
www.aitech1.ru

PEGATRON		Title : FRAME BUFFER C	
BG1-CSC-HW R&D Dept. 5		Engineer: Keyi Liu	
Size C	Project Name VGFTG	Rev 1.1	
Date: Tuesday, December 11, 2012		Sheet	96 of 104

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PEGATRON		Title : ****	
BG1-CSC-HW R&D Dept.5		Engineer: <i>Keby Liu</i>	
Size	Project Name		Rev
Custom	VGFTG		1.1
Date: <u>Tuesday, December 11, 2012</u>		Sheet	97 of 104

Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



Power On Sequence



Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]

